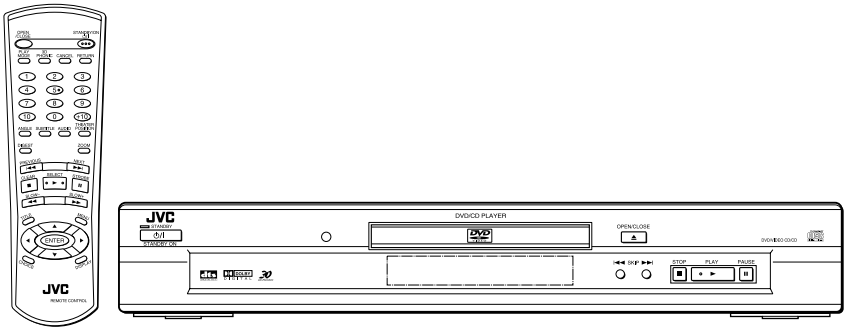
JVC

SERVICE MANUAL

DVD VIDEO PLAYER

XV-S40BK / XV-S42SL
XV-S45GD / XV-S30BK



Each difference point

Model	Body color	Optical digital out	AV Compulink
XV-S40BK	Black	O	O
XV-S42SL	Silver	O	O
XV-S45GD	Gold	O	O
XV-S30BK	Black	X	X

Area Suffix (XV-S40BK/XV-S30BK)
J ---------- U.S.A.
C ---------- Canada

Area Suffix (XV-S42SL)
C ---------- Canada

Area Suffix (XV-S45GD)
J ---------- U.S.A.

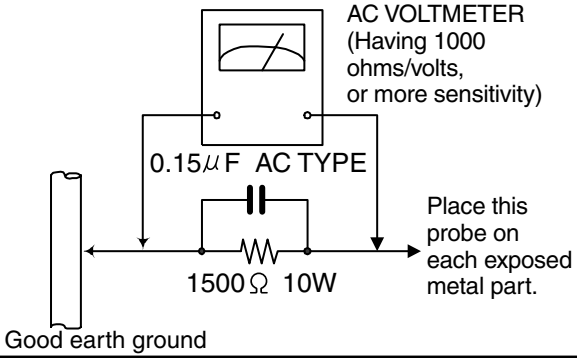
Contents

This service manual is printed on 100% recycled paper.
COPYRIGHT © 2001 VICTOR COMPANY OF JAPAN, LTD.

No.A0003
Feb. 2001

Safety Precautions

1. This design of this product contains special hardware and many circuits and components specially for safety purposes. For continued protection, no changes should be made to the original design unless authorized in writing by the manufacturer. Replacement parts must be identical to those used in the original circuits. Services should be performed by qualified personnel only.
2. Alterations of the design or circuitry of the product should not be made. Any design alterations of the product should not be made. Any design alterations or additions will void the warranty and will further relieve the manufacture of responsibility for personal injury or property damage resulting therefrom.
3. Many electrical and mechanical parts in the products have special safety-related characteristics. These characteristics are often not evident from visual inspection nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in the Parts List of Service Manual. Electrical components having such features are identified by shading on the schematics and by (⚠) on the Parts List in the Service Manual. The use of a substitute replacement which does not have the same safety characteristics as the recommended replacement parts shown in the Parts List of Service Manual may create shock, fire, or other hazards.
4. The leads in the products are routed and dressed with ties, clamps, tubings, barriers and the like to be separated from live parts, high temperature parts, moving parts and/or sharp edges for the prevention of electric shock and fire hazard. When service is required, the original lead routing and dress should be observed, and it should be confirmed that they have been returned to normal, after reassembling.
5. Leakage current check (Electrical shock hazard testing)
   After reassembling the product, always perform an isolation check on the exposed metal parts of the product (antenna terminals, knobs, metal cabinet, screw heads, headphone jack, control shafts, etc.) to be sure the product is safe to operate without danger of electrical shock.
   Do not use a line isolation transformer during this check.
   - Plug the AC line cord directly into the AC outlet. Using a "Leakage Current Tester", measure the leakage current from each exposed metal parts of the cabinet , particularly any exposed metal part having a return path to the chassis, to a known good earth ground. Any leakage current must not exceed 0.5mA AC (r.m.s.)
   - Alternate check method
     Plug the AC line cord directly into the AC outlet. Use an AC voltmeter having, 1,000 ohms per volt or more sensitivity in the following manner. Connect a 1,500Ω 10W resistor paralleled by a 0.15μF AC-type capacitor between an exposed metal part and a known good earth ground.
     Measure the AC voltage across the resistor with the AC voltmeter.
     Move the resistor connection to each exposed metal part, particularly any exposed metal part having a return path to the chassis, and measure the AC voltage across the resistor. Now, reverse the plug in the AC outlet and repeat each measurement. voltage measured Any must not exceed 0.75 V AC (r.m.s.). This corresponds to 0.5



Warning

1. This equipment has been designed and manufactured to meet international safety standards.
2. It is the legal responsibility of the repairer to ensure that these safety standards are maintained.
3. Repairs must be made in accordance with the relevant safety standards.
4. It is essential that safety critical components are replaced by approved parts.
5. If mains voltage selector is provided, check setting for local voltage.

⚠ ***CAUTION*** **Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of preforming repair of this system.**

Preventing static electricity

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs.

1.1. Grounding to prevent damage by static electricity

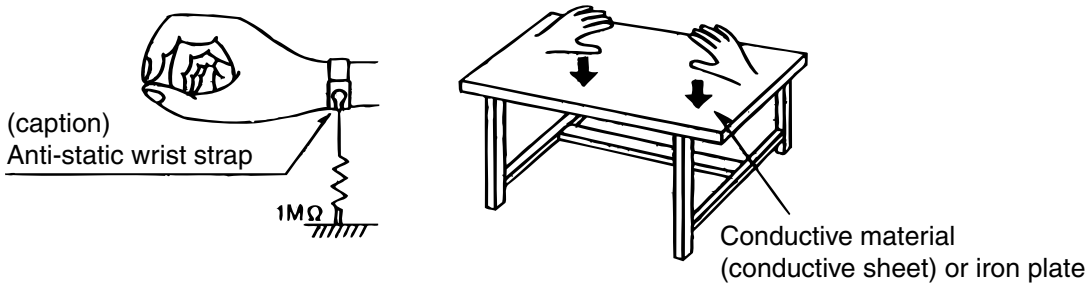
Static electricity in the work area can destroy the optical pickup (laser diode) in devices such as DVD players. Be careful to use proper grounding in the area where repairs are being performed.

1.1.1. Ground the workbench

1. Ground the workbench by laying conductive material (such as a conductive sheet) or an iron plate over it before placing the traverse unit (optical pickup) on it.

1.1.2. Ground yourself

1. Use an anti-static wrist strap to release any static electricity built up in your body.



1.1.3. Handling the optical pickup

1. In order to maintain quality during transport and before installation, both sides of the laser diode on the replacement optical pickup are shorted. After replacement, return the shorted parts to their original condition. (Refer to the text.)

2. Do not use a tester to check the condition of the laser diode in the optical pickup. The tester's internal power source can easily destroy the laser diode.

1.2. Handling the traverse unit (optical pickup)

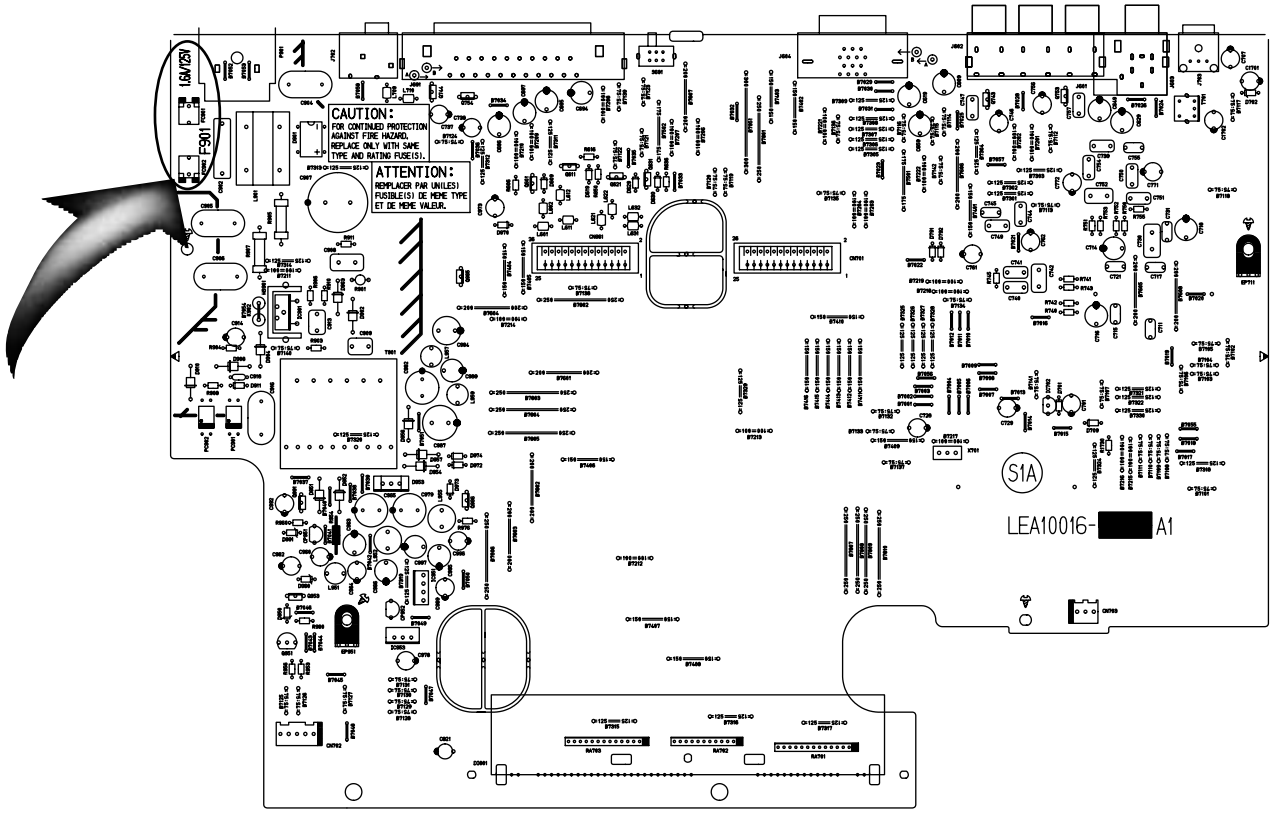
1. Do not subject the traverse unit (optical pickup) to strong shocks, as it is a sensitive, complex unit.

2. Cut off the shorted part of the flexible cable using nippers, etc. after replacing the optical pickup. For specific details, refer to the replacement procedure in the text. Remove the anti-static pin when replacing the traverse unit. Be careful not to take too long a time when attaching it to the connector.

3. Handle the flexible cable carefully as it may break when subjected to strong force.

4. It is not possible to adjust the semi-fixed resistor that adjusts the laser power. Do not turn it

Importance Admistering point on the Safety



Full Fuse Replacement Marking	Marquage Pour Le Remplacement Complet De Fusible
Graphic symbol mark (This symbol means fast blow type fuse.) should be read as follows ;	Le symbole graphique (Ce symbole signifie fusible de type á fusion rapide.) doit être interprété comme suit ;
FUSE CAUTION	**PRECAUTIONS SUR LES FUSIBLES**
FOR CONTINUED PROTECTION AGAINST RISK OF FIRE, REPLACE ONLY WITH SAME TYPE AND RATING OF FUSES ; **F901 : 1.6 A / 125 V**	**POUR UNE PROTECTION CONTINUE CONTRE DES RISQUES D'INCENDIE, REMPLACER SEULEMENT PAR UN FUSIBLE DU MEME TYPE ;** **F901 : 1.6 A / 125 V**

Precautions for Service

Handling of Traverse Unit and Laser Pickup

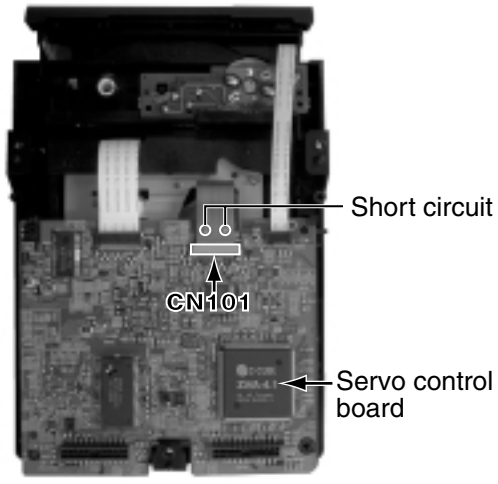
1. Do not touch any peripheral element of the pickup or the actuator.
2. The traverse unit and the pickup are precision devices and therefore must not be subjected to strong shock.
3. Do not use a tester to examine the laser diode. (The diode can easily be destroyed by the internal power supply of the tester.)
4. To replace the traverse unit, pull out the metal short pin for protection from charging.
5. When replacing the pickup, after mounting a new pickup, remove the solder on the short land which is provided at the center of the flexible wire to open the circuit.
6. Half-fixed resistors for laser power adjustment are adjusted in pairs at shipment to match the characteristics of the optical block.
   Do not change the setting of these half-fixed resistors for laser power adjustment.

Destruction of Traverse Unit and Laser Pickup by Static Electricity

Laser diodes are easily destroyed by static electricity charged on clothing or the human body. Before repairing peripheral elements of the traverse unit or pickup, be sure to take the following electrostatic protection:

1. Wear an antistatic wrist wrap.
2. With a conductive sheet or a steel plate on the workbench on which the traverse unit or the pick up is to be repaired, ground the sheet or the plate.
3. After removing the flexible wire from the connector (CN101), short-circuit the flexible wire by the metal clip.
4. Short-circuit the laser diode by soldering the land which is provided at the center of the flexible wire for the pickup.
   After completing the repair, remove the solder to open the circuit.

Please refer to "Fig.4" of "Disassembly method" for details.



Disassembly method

<Main body>

■ Removing the top cover (see Fig.1)

1.Remove the two screws **A** attaching the top cover on both sides of the body.

2.Remove the three screws **B** attaching the top cover on the back of the body.

3.Remove the top cover from the body by lifting the rear part of the top cover.

ATTENTION: Do not break the front panel tab fitted to the top cover.

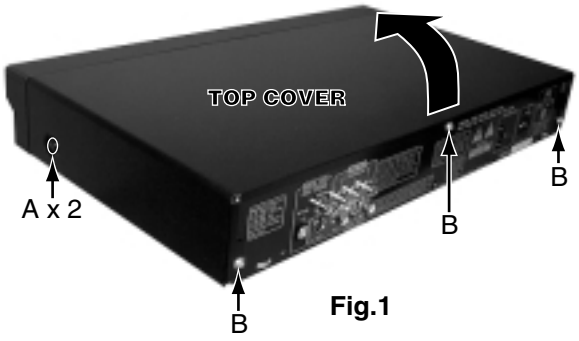


Fig.1

■ Removing the mechanism assembly (see Fig.2,3)

* Prior to performing the following procedure, remove the top cover.
* There is no need to remove the front panel assembly.

1.Remove the three screws **C** attaching the mechanism assembly on the bottom chassis.

2.The servo control board is removed from the connector CN961 and CN701 connected with the main board respectively.

3.Remove the mechanism assembly by lifting the rear part of the mechanism assembly.

*Please remove lug wire when you do not remove the mechanism assembly easily.

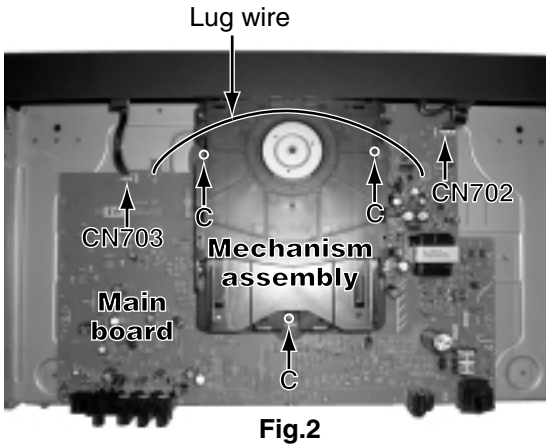


Fig.2

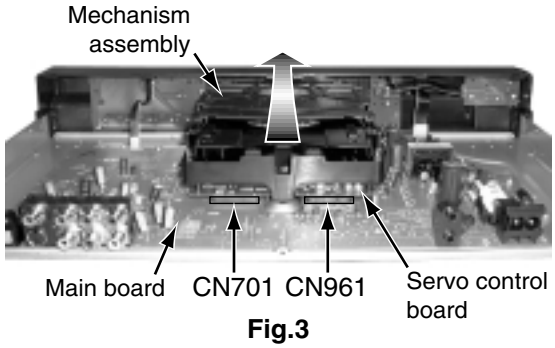


Fig.3

■ Removing the servo control board (see Fig.4)

* Prior to performing the following procedure, remove the top cover and mechanism assembly.

1.Disconnect the card wire from connector CN201 and CN202 on the servo control board respectively.

2.Disconnect the flexible wire from connector CN101 on the servo control board from pick-up.

ATTENTION
At this time, please extract the wire after short-circuited of two places on the wire in part **a** with solder.
Please remove the solder two places of part **a** after connecting the wire with CN101 when reassembling.

3.Two places in hook **b** are removed, the servo control board is lifted, and it is removed.

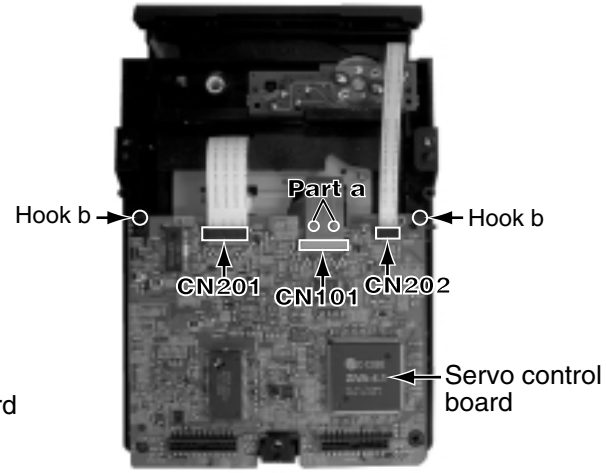


Fig.4

■ Removing the rear panel (see Fig.5)

*Prior to performing the following procedure, remove the top cover.

1.Remove the six screws **D** attaching the rear panel on the back of the body.

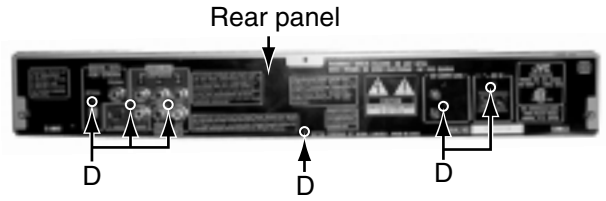


Fig.5

■ Removing the front panel assembly (see Fig.6,7)

* Prior to performing the following procedure, remove the top cover.
* There is no need to remove the mechanism assembly.

1.Remove the one screw **E** attaching the front panel assembly on the bottom chassis.

2.Disconnect the wire from CN702 and CN703 on the main board respectively.

3.Hook **c** and **d** are removed respectively, and the front panel assembly is removed.

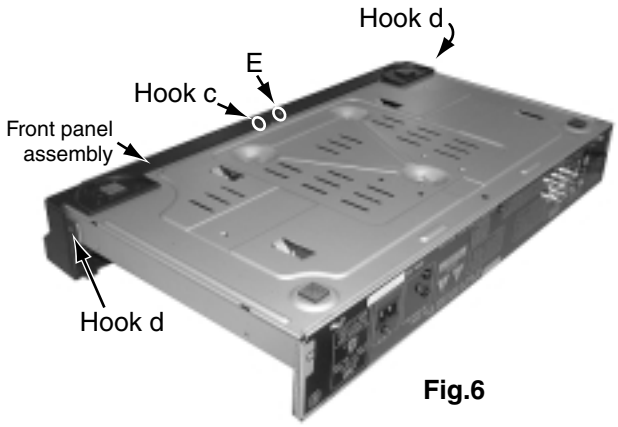


Fig.6

■ Removing the main board (see Fig.8)

* Prior to performing the following procedure, remove the top cover, mechanism assembly and rear panel.

1.Disconnect the wire from CN702 and CN703 on the main board respectively.

2.Remove the four screws **F** attaching the main board on the bottom chassis.

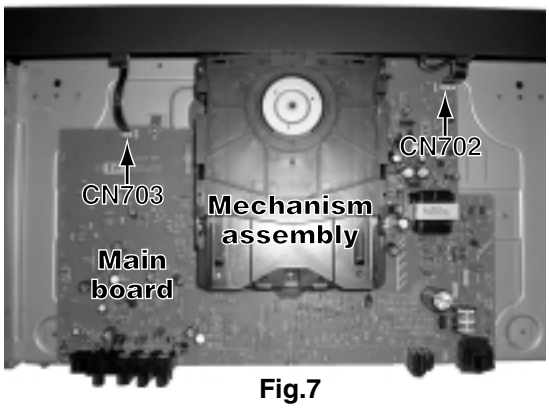


Fig.7

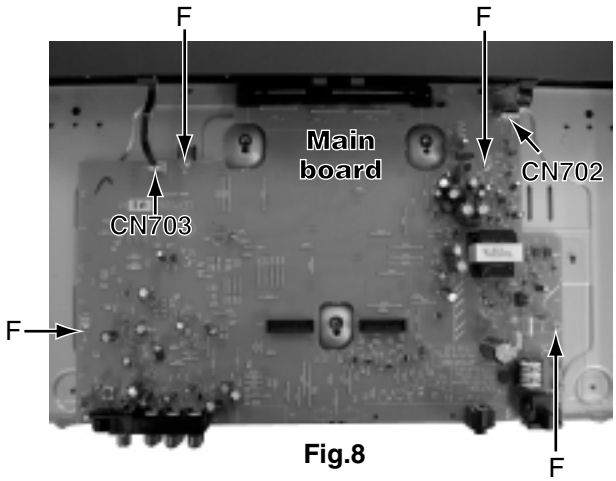


Fig.8

<Loading assembly section>

■ Removing the clamper assembly (See Fig.1)

1. Remove the four screws **A** attaching the clamper assembly.

2. Move the clamper in the direction of the arrow to release the two joints **a** on both sides.

ATTENTION: When reattaching, fit the clamper to the two joints **a**.

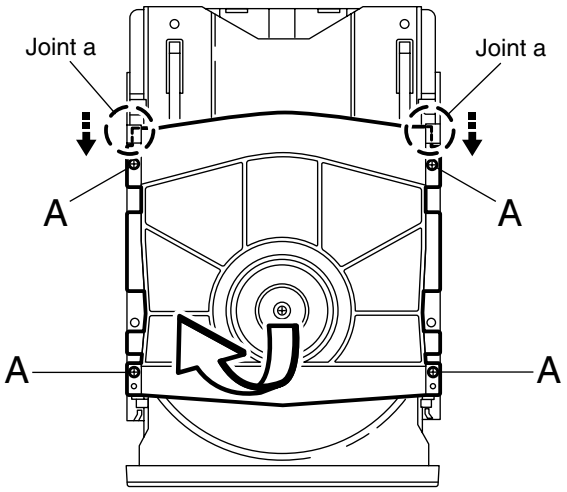


Fig.1

■ Removing the tray (See Fig.2 and 3)

・ Prior to performing the following procedure, remove the clamper assembly.

1. Push **b** of the slide cam into the slot on the left side of the loading base until it stops.

2. Draw out the tray toward the front.

ATTENTION: Before reattaching the tray, slide the part **c** of the slide cam to the right as shown in Fig.3.

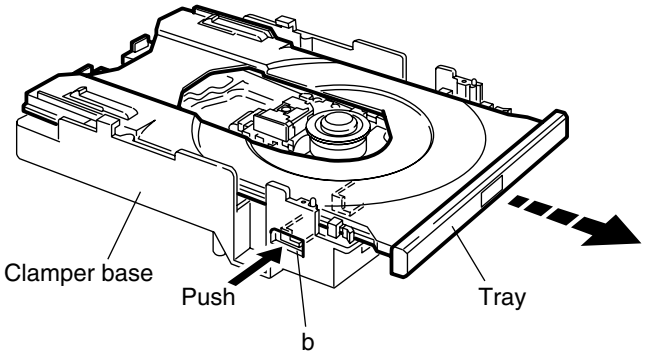


Fig.2

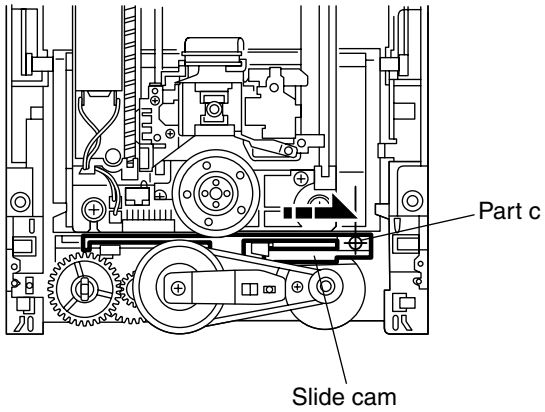


Fig.3

■Removing the traverse mechanism assembly (See Fig.4 and 5)

・ Prior to performing the following procedure, remove the clamper assembly and the tray.

1. Remove the four screws **B** attaching the traverse mechanism assembly.

ATTENTION: Before reattaching the traverse mechanism assembly, pass the card wire extending from the spindle motor board through the notch **d** of the elevator.

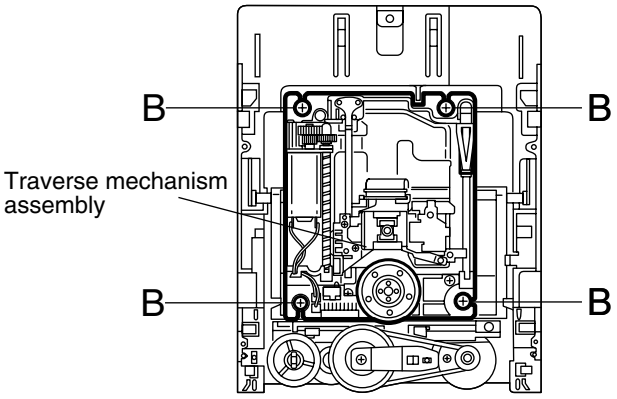


Fig.4

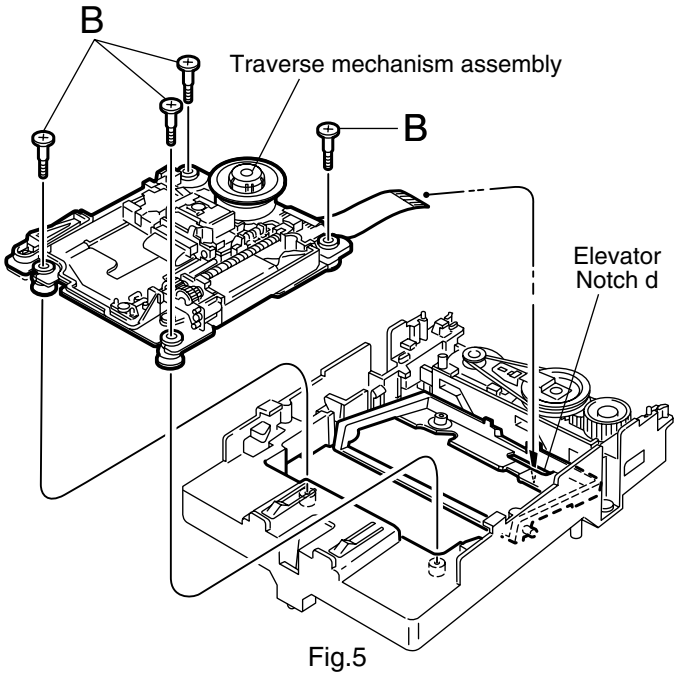


Fig.5

■Removing the elevator (See Fig.6 and 7)

・ Prior to performing the following procedure, remove the clamper assembly, the tray and the traverse mechanism assembly.

1. Extend each bar **e** inside of the loading base outward and detach the elevator shaft.

ATTENTION: When reattaching, first fit the two shafts on the front of the elevator to the slots **f** of the slide cam.

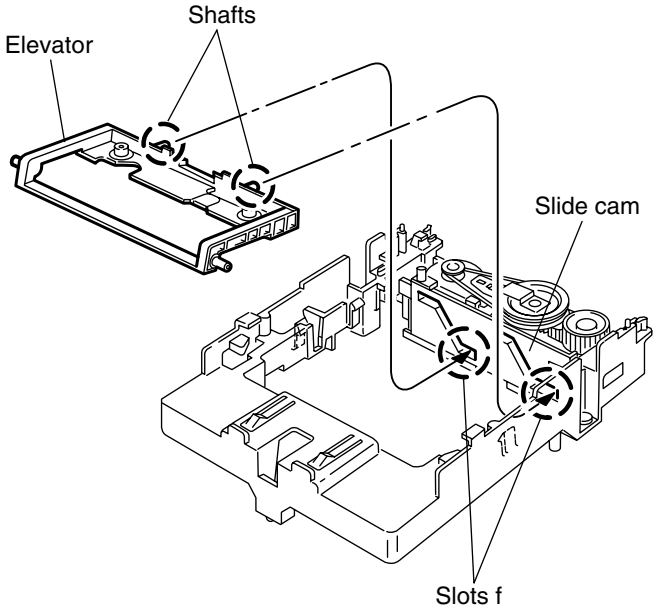


Fig.7

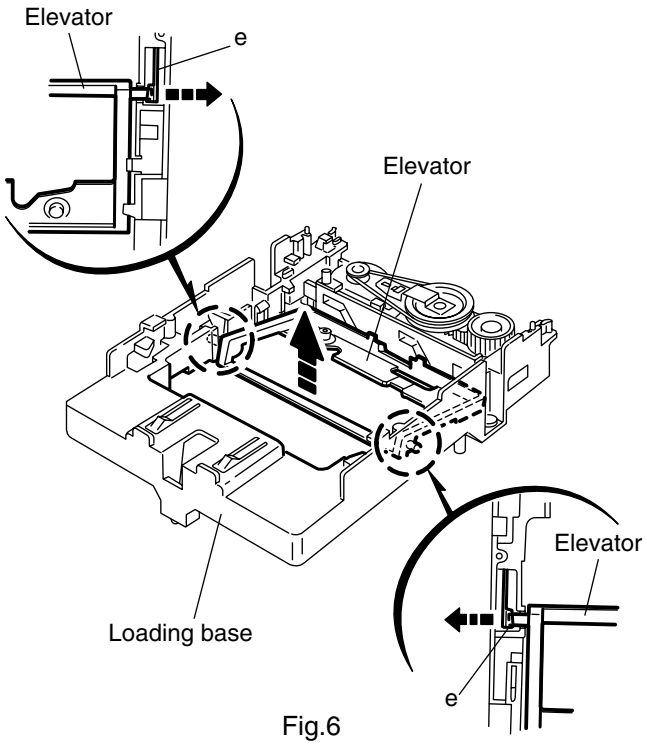


Fig.6

■ Removing the motor assembly (See Fig.8 and 9)

- Prior to performing the following procedure, remove the clamper assembly, the tray, the traverse mechanism assembly and the elevator.

1. Remove the belt from the pulley.
2. Remove the screw **C** attaching the motor assembly.
3. Turn over the body and remove the screw **D** attaching the motor assembly.
4. Release the two tabs **g** retaining the motor board.

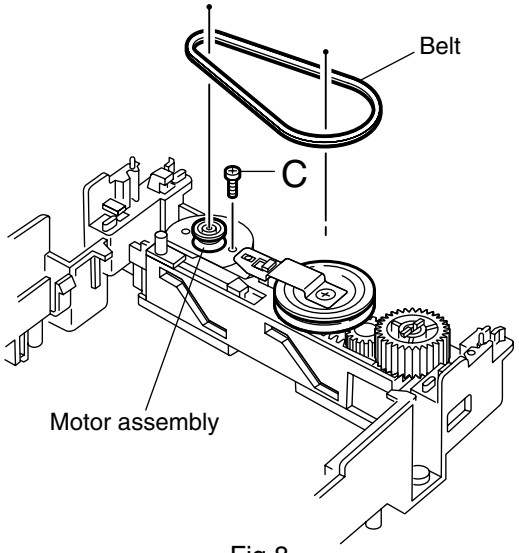


Fig.8

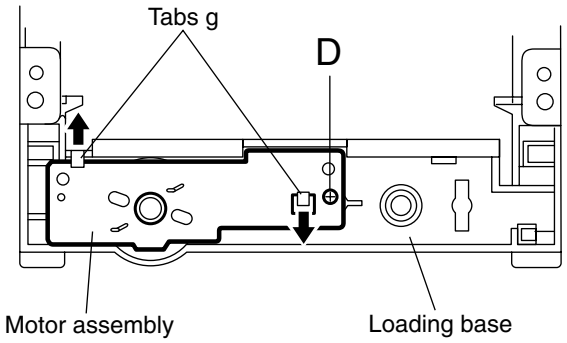


Fig.9

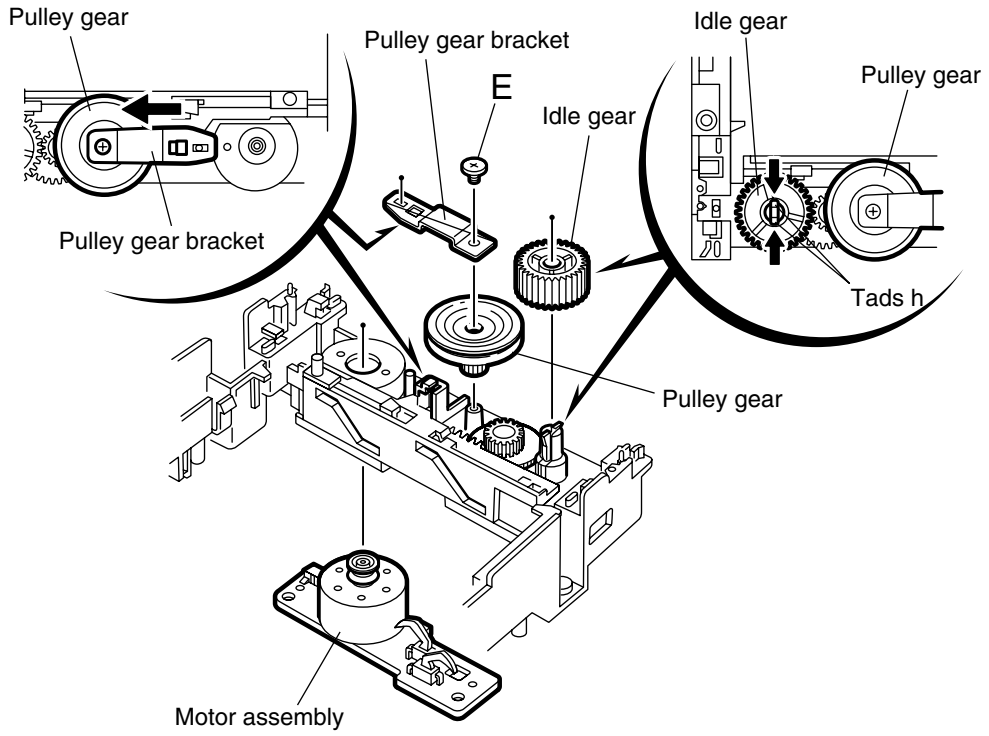


Fig.10

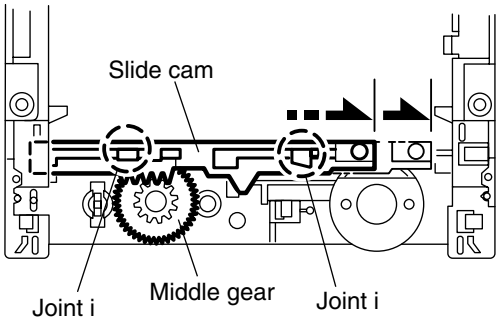


Fig.11

■Removing the Idle gear / pulley gear / middle gear / slide cam (See Fig.10 to 12)

・ Prior to performing the following procedure, remove the clamper assembly, the tray, the traverse mechanism assembly, the elevator and the motor assembly.

1. Press the two tabs **h** inward and pull out the idle gear.

2. Remove the screw **E** attaching the pulley gear bracket. Slide the pulley gear bracket in the direction of the arrow and pull out the pulley gear.

3. Slide the slide cam in the direction of the arrow to release the two joints **i** and remove upward.

4. Remove the middle gear.

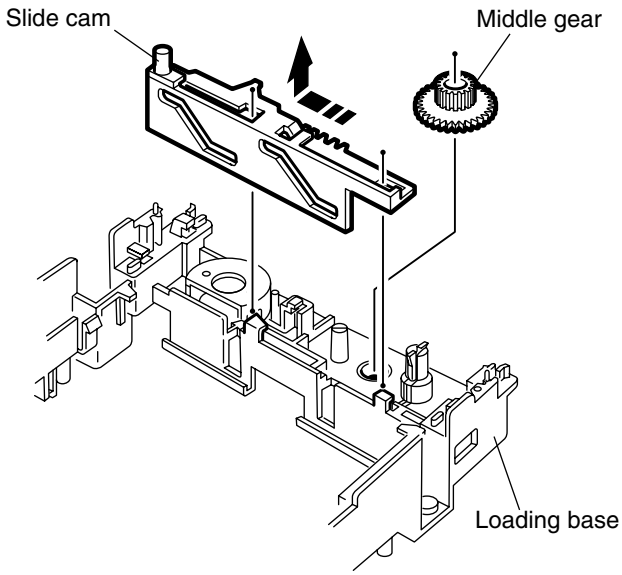


Fig.12

<Traverse mechanism assembly section>

■ Removing the feed motor assembly (See Fig.13)

1. Unsolder the two soldering **j** on the spindle motor board.

2. Remove the two screws **F** attaching the feed motor assembly.

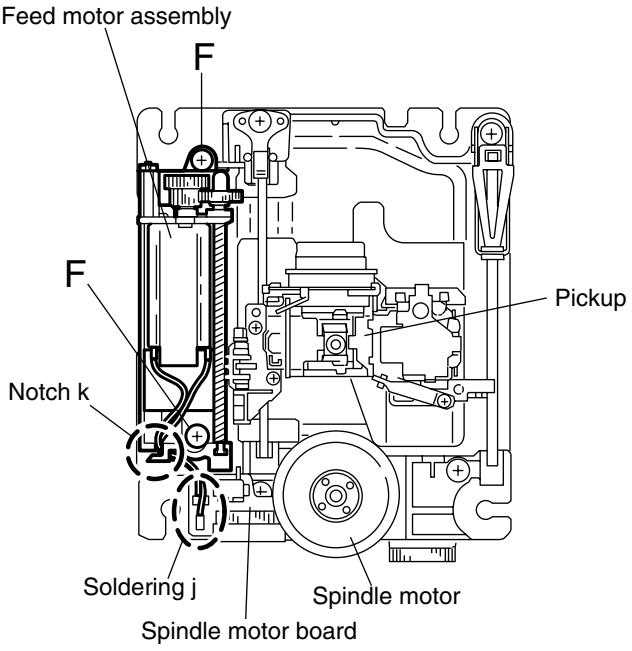


Fig.13

■ Removing the feed motor (See Fig.13 to 15)

・ Prior to performing the following procedure, remove the feed motor assembly.

1. Remove the screw **G** attaching the thrust spring.

ATTENTION: When reattaching the thrust spring, make sure that the thrust spring presses the feed gear (M) and the feed gear (E) reasonably.

2. Remove the feed gear (M).

3. Pull out the feed gear (E) and the lead screw.

4. Remove the two screws **H** attaching the feed motor.

ATTENTION: When reattaching, pass the two cables extending from the feed motor through the notch **k** of the feed holder as shown in Fig.13.

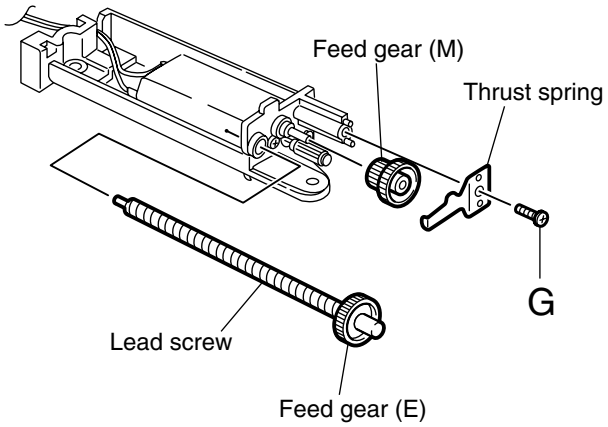


Fig.14

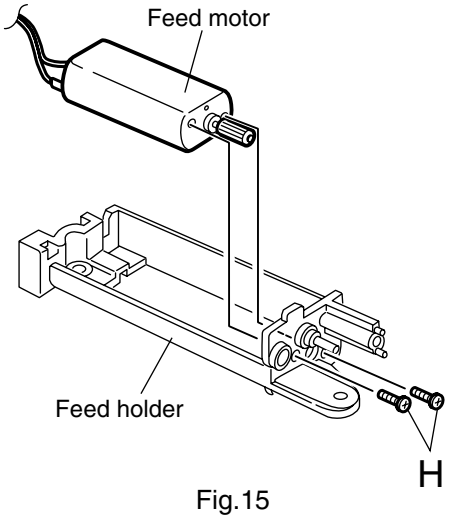


Fig.15

■ Removing the pickup (See Fig.16 and 17)

1. Remove the screw **l** attaching the T spring (S) and the shaft holder. Remove also the plate.

ATTENTION: When reattaching, make sure that the T spring (S) presses the shaft.

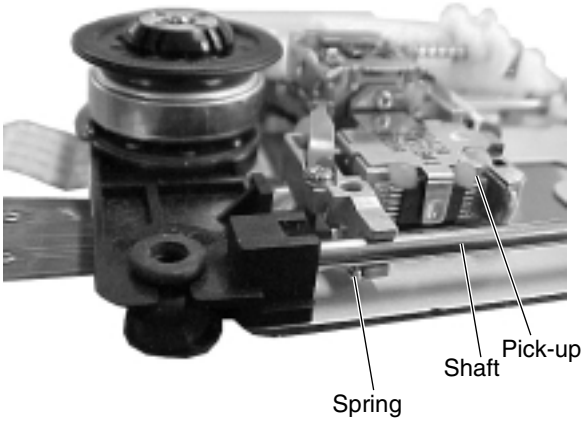
2. Pull out the part **l** of the shaft upward. Move the part **m** in the direction of the arrow and detach from the spindle base.

3. Disengage the joint **n** of the pickup and the shaft in the direction of the arrow.

4. Pull out the shaft from the pickup.

5. Remove the two screws **J** attaching the actuator.

6. Disengage the joint of the actuator and the lead spring. Pull out the lead spring.



The spring must be under the shaft when you install pick-up.

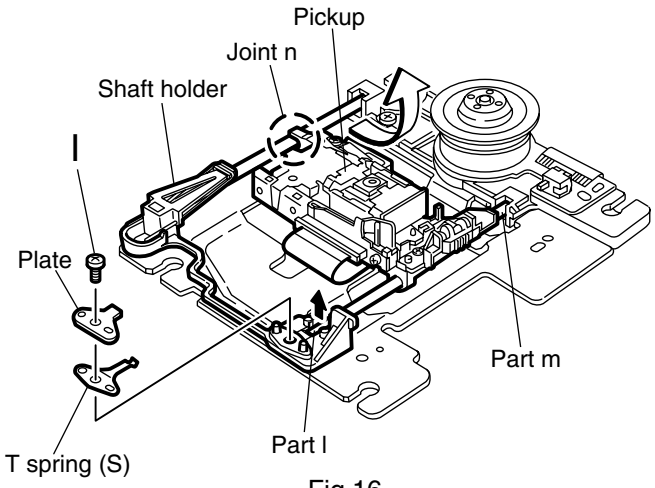


Fig.16

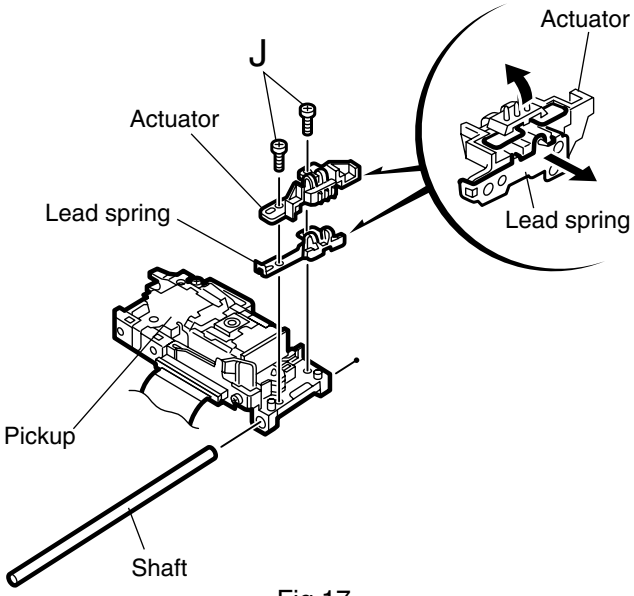


Fig.17

■ Removing the shaft holder / shaft (See Fig.18)

1. Remove the screw **K** attaching the shaft holder.

2. Remove the shaft.

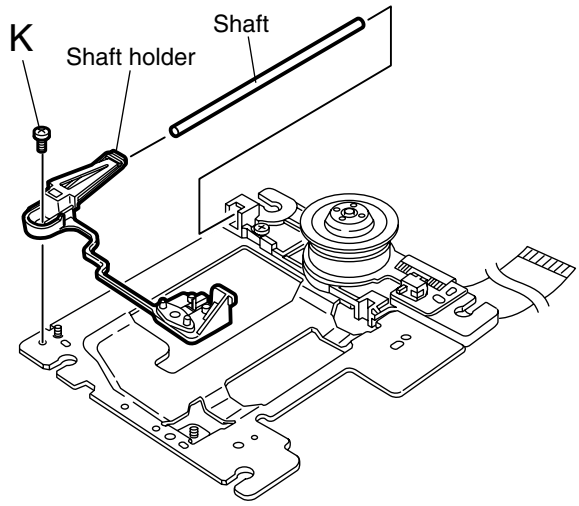


Fig.18

■ Removing the spindle motor assembly (See Fig.19 to 21)

1. Remove the three screws **L** attaching the spindle motor on the bottom of the mechanism base.

ATTENTION: When reattaching, pass the card wire extending from the spindle motor board through the notch of the spindle base.

2. Remove the three screws **M** attaching the spindle base.

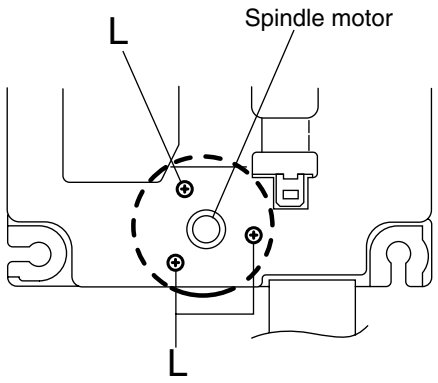


Fig.19

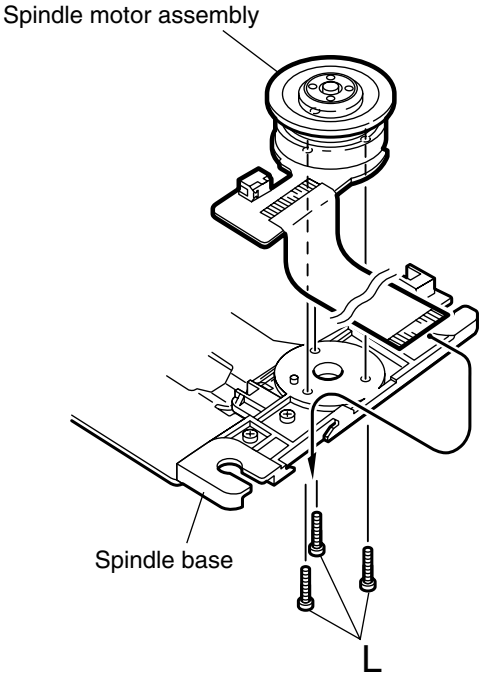


Fig.20

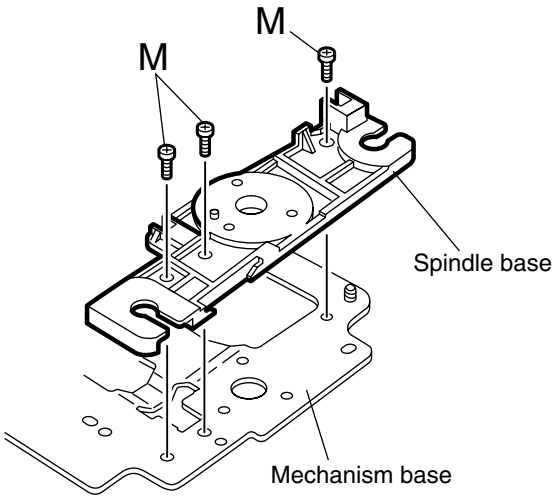


Fig.21

Adjustment method

(1) Initialization method

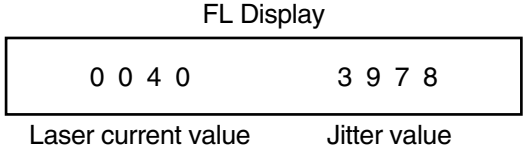
If microprocessor (IC401,IC402,IC403) or pick-up is replaces, initialize the DVD player in the following matter

1)Take out the disc and close the tray.
2)Unplug the power plug.
3)Insert power plug into outlet while pressing both PLAY button and OPEN/CLOSE button.
4)FL Display indicate "TEST ＊＊　¥" .　＊＊ :Version,　　¥:Region code
5)Press 3D-PHONIC key button of remote controller. and EEPROM initialize start.
6)When indicate "DTS" on the display, initialize finishes.
7)The power is turned OFF, and Unplug the power plug.

(2) Display of "Laser current value" and "Jitter value"

"Laser current value" and "Jitter value" are displayed on the FL display by the undermentioned method. Please refer to the failure diagnosis.

1)Take out the disc and close the tray.
2)Unplug the power plug.
3)Insert power plug into outlet while pressing both PLAY button and OPEN/CLOSE button.
4)FL Display indicate "TEST ＊＊　¥" .　＊＊ :Version,　　¥:Region code
5)Press the "OPEN/CLOSE" button to move the tray outward.
Put the test disc (VT-501) on the tray and press "OPEN/CLOSE" button.
The tray should move inward (Note:Don't push to close the tray directly by hand etc.)
6)Press the "PLAY" button.
7)The laser current value and the jitter value is displayed on the FL indicator as follows.



* The test mode is canceled when the power is turned off.

■ For Laser current value

The laser current value becomes 40mA for the above-mentioned.
Becomes a test mode by doing above-mentioned procedure 1) - 4). Afterwards, the laser current value can be switched by pushing the key to remote control without turning on the disk.

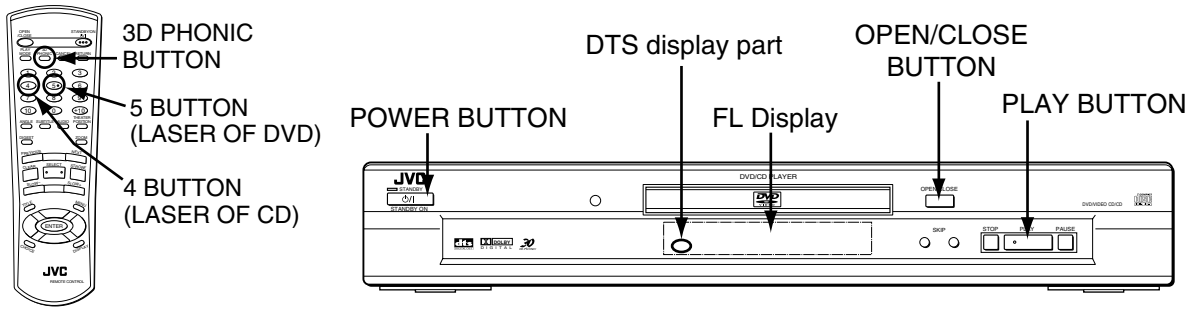
Remote control "4" key --- Laser of CD
Remote control "5" key --- Laser of DVD

*Returns to a usual test mode by the thing to push the stop button of remote control.

If the laser current value is 64mA or less, it is roughly good. There is a possibility to which pick-up is deteriorated, and exchange pick-up, please when there are 65mA or more laser current value.

■ For Jitter value

The jitter value is displayed by the hexadecimal number and refer to the conversion table of following,please.
If the indication value is 11% or less, it can be judged by this simple checking method that the signal read precision of the set is satisfactory.
Before using the TEST disc VT-501, careful check it if there is neither damage nor dirt on the read surface.



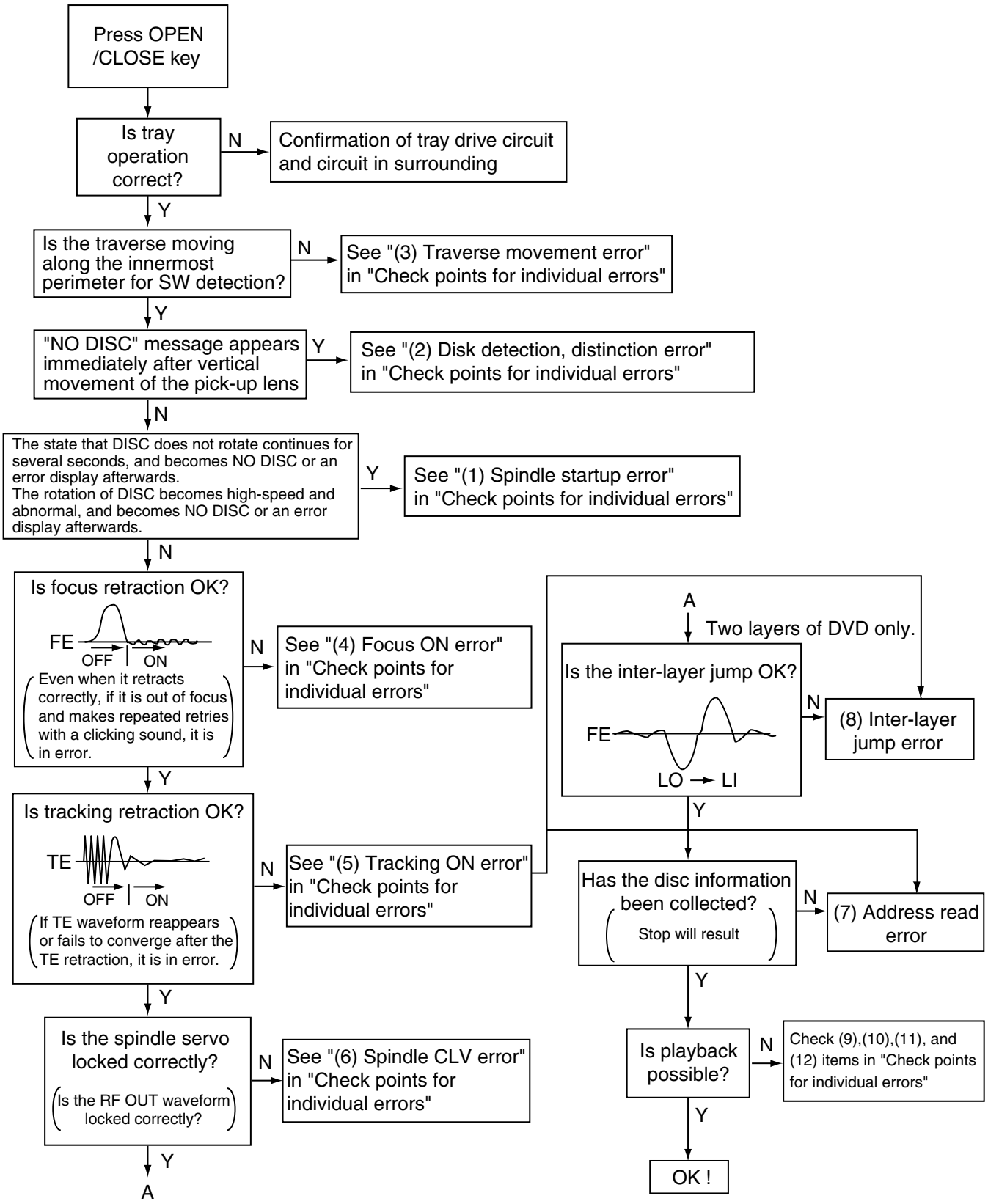
■ Jitter value

FL display	Conversion value(&)	FL display	Conversion value(&)
3818	4.7	3998	7.6
3828	4.8	39A8	7.7
3838	4.9	39B8	7.8
3848	5.1	39C8	7.9
3858	5.2	39D8	8.1
3868	5.3	39E8	8.2
3878	5.4	39F8	8.3
3888	5.5	3A18	8.5
3898	5.7	3A28	8.7
38A8	5.8	3A38	8.8
38b8	5.9	3A48	8.9
38c8	6.0	3A58	9.0
38d8	6.1	3A68	9.1
38E8	6.3	3A78	9.3
38F8	6.4	3A88	9.4
3918	6.6	3A98	9.5
3928	6.7	3AA8	9.6
3938	6.9	3AB8	9.7
3948	7.0	3AC8	9.9
3958	7.1	3AD8	10.0
3968	7.2	3AE8	10.1
3978	7.3	3AF8	10.2
3988	7.5		

FL display	Conversion value(&)	FL display	Conversion value(&)
3B18	10.5	3C98	13.3
3B28	10.6	3CA8	13.5
3B38	10.7	3CB8	13.6
3B48	10.8	3CC8	13.7
3B58	10.9	3CD8	13.8
3B68	11.1	3CE8	13.9
3B78	11.2	3CF8	14.1
3B88	11.3	3D18	14.3
3B98	11.4	3D28	14.4
3BA8	11.5	3D38	14.5
3BB8	11.7	3D48	14.7
3BC8	11.8	3D58	14.8
3BD8	11.9	3D68	14.9
3BE8	12.0	3D78	15.0
3BF8	12.1	3D88	15.1
3C18	12.4	3D98	15.3
3C28	12.5	3DA8	15.4
3C38	12.7	3DB8	15.5
3C48	12.7	3DC8	15.6
3C58	12.9	3DD8	15.7
3C68	13.0	3DE8	15.9
3C78	13.1	3DF8	16.0
3C88	13.2		

Troubleshooting

Servo volume



Check points for each error

(1) Spindle start error

1.Defective spindle motor

*Are there several ohms resistance between each pin of CN201 "5-6","6-7","5-7"?
(The power supply is turned off and measured.)

*Is the sign wave of about 100mVp-p in the voltage had from each terminal?
[CN201"9"(H1-),"10"(H1+),"11"(H2-),"12"(H2+),"13"(H3-),"14"(H3+)]

2.Defective spindle motor driver (IC251)

*Has motor drive voltage of a sine wave or a rectangular wave gone out to each terminal(SM1~3)
of CN201"5,6,7" and IC251"2,4,7"?

*Is FG pulse output from the terminal of IC251"24"(FG) according to the rotation of the motor?

*Is it "L(about 0.9V)" while terminal of IC251"15"(VH) is rotating the motor?

3.Has the control signal come from servo IC or the microcomputer?

*Is it "L" while the terminal of IC251"16"(SBRK) is operating?
Is it "H" while the terminal of IC251"23"(/SPMUTE) is operating?

*Is the control signal input to the terminal of IC251"22"(EC)?
(changes from VHALF voltage while the motor is working.)

*Is the VHALF voltage input to the terminal of IC251"21"(ECR)?

4.Is the FG signal input to the servo IC?

*Is FG pulse input to the terminal of IC201"53"(FG) according to the rotation of the motor?

(2) Disc Detection, Distinction error (no disc, no RFENV)

* Laser is defective.
* Front End Processor is defective (IC101).
* APC circuit is defective. --- Q101,Q102.
* Pattern is defective. --- Lines for CN101 - All patterns which relate to pick-up and patterns between IC101
* Servo IC is defective (IC201).
* IC101 --- For signal from IC101 to IC201, is signal output from IC101 "20" (ASOUT) and
IC101 "41"(RFENV) and IC101 "22" (FEOUT)?

(3) Traverse movement NG

1.Defective traverse driver
*Has the voltage come between terminal of CN101 "1" and "2" ?

2.Defective BTL driver (IC271)
*Has the motor drive voltage gone out to IC271"17" or "18"?

3.Has the control signal come from servo IC or the microcomputer?
*Is it "H" while the terminal of IC271"9"(STBY1) ?
*TRSDRV Is the signal input?

4.TRVSW is the signal input from microcomputer?

(4) Focus ON NG

* Is FE output ? --- Pattern, IC101
* Is FODRV signal sent ? (R279) --- Pattern, IC201
* Is driving voltage sent ?
  IC271 "13", "14" --- If NG, pattern, driver, mechanical unit .
* Mechanical unit is defective.

(5) Tracking ON NG

* When the tracking loop cannot be drawn in, TE shape of waves does not settle.
* Mechanical unit is defective.
  Because the self adjustment cannot be normally adjusted, the thing which cannot be normally drawn in is thought.
* Periphery of driver (IC271)
  Constant or IC it self is defective.
* Servo IC (IC201)
  When improperly adjusted due to defective IC.

(6) Spindle CLV NG

* IC101 -- "35"(RF OUT), "30"(RF-), "31(RF+).
* Does not the input or the output of driver's spindle signal do the grip?
* Has the tracking been turned on?
* Spindle motor and driver is defective.
* Additionally, "IC101 and IC201" and "Mechanism is defective(jitter)", etc. are thought.

(7) Address read NG

* Besides, the undermentioned cause is thought though specific of the cause is difficult because various factors are thought.
  Mechanism is defective. (jitter)
  IC201, IC301, IC401.
  The disc is dirty or the wound has adhered.

(8) Between layers jump NG (double-layer disc only)

Mechanism defective
Defect of driver's IC(IC271)
Defect of servo control IC(IC201)

(9) Neither picture nor sound is output

1.It is not possible to search
*Has the tracking been turned on?
*To "(5) Tracking ON error" in "Check points for individual errors" when the tracking is not normal.
*Is the feed operation normal?
To "(3) traverse movement NG" in "Check points for individual errors" when it is not normal.
Are not there caught of the feeding mechanism etc?

(10) Picture is distorted or abnormal sound occurs at intervals of several seconds.

Is the feed operation normal?
Are not there caught of the feeding mechanism etc?

(11) Others

The image is sometimes blocked, and the image stops.
The image is blocked when going to outer though it is normal in surroundings in the disk and the stopping symptom increases.

} There is a possibility with bad jitter value for such a symptom.

(12) CD During normal playback operation

a) Is TOC reading normal?
Displays total time for CD-DA.
Shifts to double-speed mode for V-CD.

↓ YES

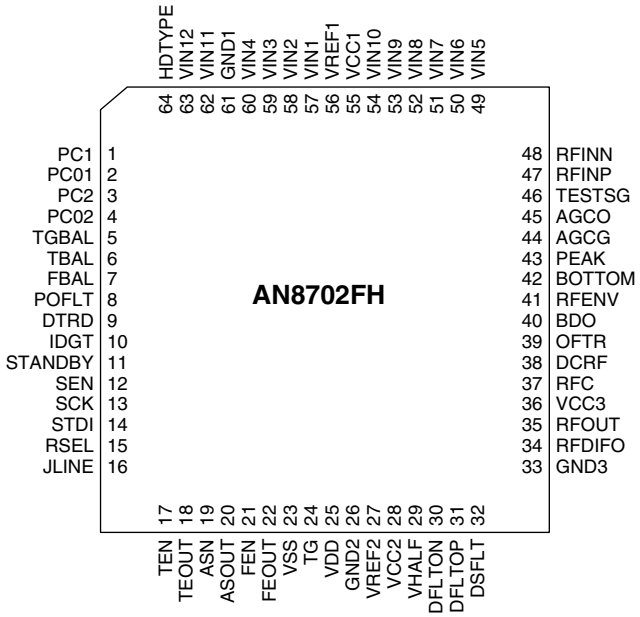
b)Playback possible? → NO

*--:-- is displayed during FL search.
According to [It is not possible to search] for DVD(9), check the feed and tracking systems.
*No sound is output although the time is displayed.(CA-DA)
DAC, etc, other than servo.
*The passage of time is not stable, or picture is abnormal.(V-CD)
*The wound of the disc and dirt are confirmed.

Description of major ICs

■ AN8702FH(IC101):Frontend processor

1.Pin layout

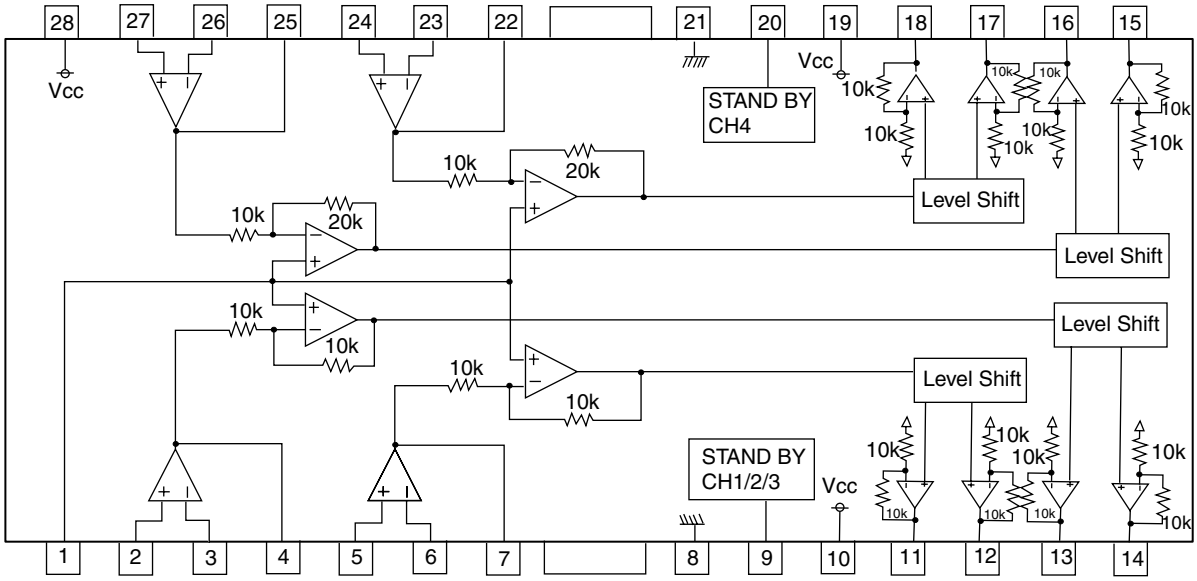


2.Pin function

Pin No.	Symbol	I/O	Description	Pin No.	Symbol	I/O	Description
1	PC1			34	RFDIFO		
2	PC01			35	RFOUT		
3	PC2			36	VCC3	-	Power supply terminal 5V
4	PC02			37	RFC		
5	TGBAL	I	Tangential phase balance control terminal	38	DCRF	O	All addition amplifier capacitor terminal
6	TBAL	I	Tracking balance control terminal	39	OFTR	O	OFTR output terminal
7	FBAL	I	Focus balance control terminal	40	BDO		
8	POFLT	O	Track detection threshold level terminal	41	RFENV	O	RF envelope output terminal
9	DTRD	I	Data slice part data read signal input terminal	42	BOTTOM	O	Bottom envelope detection filter terminal
			(For RAM)	43	PEAK	O	Peak envelope detection filter terminal
10	IDGT	I	Data slice part address part gate signal input	44	AGCG	O	AGC amplifier gain control terminal
			terminal(For RAM)	45	AGCO		
11	STANDBY	I	Standby mode control terminal	46	TESTSG	I	TEST signal input terminal
12	SEN	I	SEN(Serial data input terminal)	47	RFINP	I	RF signal positive input terminal
13	SCK	I	SCK(Serial data input terminal)	48	RFINN	I	RF signal negative input terminal
14	STDI	I	STDI(Serial data input terminal)	49	VIN5	I	Focus input of external division into two terminal
15	RSEL			50	VIN6	I	Focus input of external division into two terminal
16	JLINE			51	VIN7	I	
17	TEN			52	VIN8	I	
18	TEOUT	O	Tracking error signal output terminal	53	VIN9	I	
19	ASN			54	VIN10	I	
20	ASOUT			55	VCC1	-	Power supply terminal 5V
21	FEN	I	Focus error output amplifier reversing input terminal	56	VREF1	O	VREF1 voltage output terminal
22	FEOUT	O	Focus error signal output terminal	57	VIN1	I	External division into four (DVD/CD) RF input
23	VSS	-	Connect to GND				terminal1
24	TG	O	Tangential phase error signal output terminal	58	VIN2	I	External division into four (DVD/CD) RF input
25	VDD	-	Power supply terminal 3V				terminal2
26	GND2	-	Connect to GND	59	VIN3	I	External division into four (DVD/CD) RF input
27	VREF2	O	VREF2 voltage output terminal				terminal3
28	VCC2	-	Power supply terminal 5V	60	VIN4	I	External division into four (DVD/CD) RF input
29	VHALF	O	VHALF voltage output terminal				terminal4
30	DFLTON			61	GND1	-	Connect to GND
31	DFLTOP			62	VIN11	I	
32	DSFLT			63	VIN12	I	
33	GND3	-	Connect to GND	64	HDTYPE		

■ BA5983FM-X (IC271) : 4CH DRIVER

1.Block Diagram

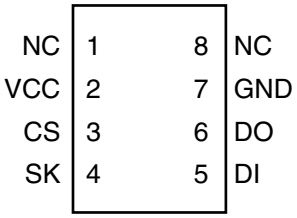


2.Pin Function

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	BIAS IN	I	Input for Bias-amplifier	15	VO4(+)	O	Non inverted output of CH4
2	OPIN1(+)	I	Non inverting input for CH1 OP-AMP	16	VO4(-)	O	Inverted output of CH4
3	OPIN1(-)	I	Inverting input for CH1 OP-AMP	17	VO3(+)	O	Non inverted output of CH3
4	OPOUT1	O	Output for CH1 OP-AMP	18	VO3(-)	O	Inverted output of CH3
5	OPIN2(+)	I	Non inverting input for CH2 OP-AMP	19	PowVcc2	-	Vcc for CH3/4 power block
6	OPIN2(-)	I	Inverting input for CH2 OP-AMP	20	STBY2	I	Input for Ch4 stand by control
7	OPOUT2	O	Output for CH2 OP-AMP	21	GND	-	Substrate ground
8	GND	-	Substrate ground	22	OPOUT3	O	Output for CH3 OP-AMP
9	STBY1	I	Input for CH1/2/3 stand by control	23	OPIN3(-)	I	Inverting input for CH3 OP-AMP
10	PowVcc1	-	Vcc for CH1/2 power block	24	OPIN3(+)	I	Non inverting input for CH3 OP-AMP
11	VO2(-)	O	Inverted output of CH2	25	OPOUT4	O	Output for CH4 OP-AMP
12	VO2(+)	O	Non inverted output of CH2	26	OPIN4(-)	I	Inverting input for CH4 OP-AMP
13	VO1(-)	O	Inverted output of CH1	27	OPIN4(+)	I	Non inverting input for CH4 OP-AMP
14	VO1(+)	O	Non inverted output of CH1	28	PreVcc	-	Vcc for pre block

■ BR93LC66F-X(IC403):EEPROM

1.Terminal layout

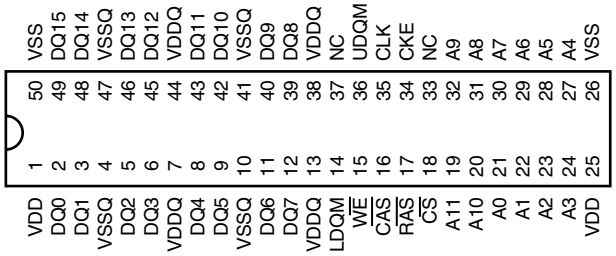


2.Pin Functions

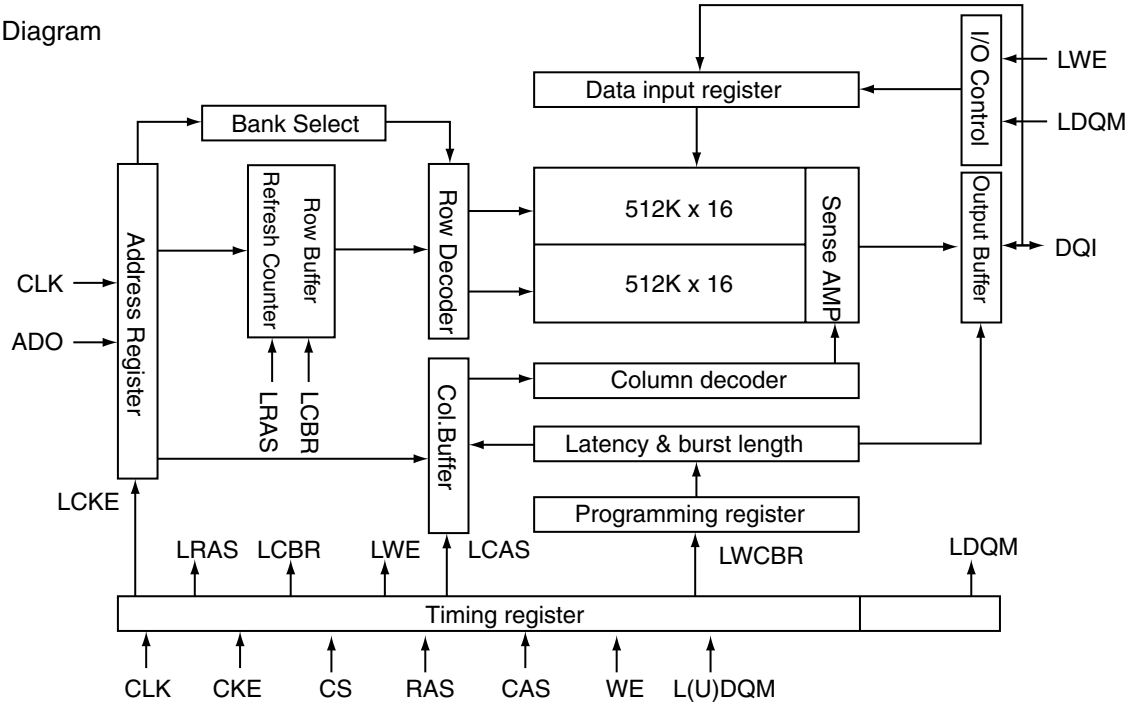
Symbol	I/O	Function
VCC	-	Power supply
GND	-	Connect to GND
CS	I	Chip select input
SK	I	Serial clock input
DI	I	Start bit,OP-code,address,serial data input
DO	O	Serial data output, Internal state display output of READY/BUSY

■ KM416S1120DT-G8(IC504,IC505):DRAM

1.Terminal Layout



2.Block Diagram



3.Pin Function

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	VDD	Power Supply	26	VSS	To Ground
2	DQ0	Data Input/Output	27	A4	Address
3	DQ1	Data Input/Output	28	A5	Address
4	VSSQ	To Ground	29	A6	Address
5	DQ2	Data Input/Output	30	A7	Address
6	DQ3	Data Input/Output	31	A8	Address
7	VDDQ	Power Supply	32	A9	Address
8	DQ4	Data Input/Output	33	NC	Non Connection
9	DQ5	Data Input/Output	34	CKE	Clock Enable
10	VSSQ	To Ground	35	CLK	System Clock
11	DQ6	Data Input/Output	36	UDOM	Data Input/Mask Output
12	DQ7	Data Input/Output	37	NC	Non Connection
13	VDDQ	Power Supply	38	VDDQ	Power Supply
14	LDQM	Data Input/Mask Output	39	DQ8	Data Input/Output
15	$\overline{WE}$	Write Enable	40	DQ9	Data Input/Output
16	$\overline{CAS}$	Column Address Strobe	41	VSSQ	To Ground
17	$\overline{RAS}$	Raw Address Strobe	42	DQ10	Data Input/Output
18	$\overline{CS}$	Chip Select	43	DQ11	Data Input/Output
19	A11	Address	44	VDDQ	Power Supply
20	A10	Address	45	DQ12	Data Input/Output
21	A0	Address	46	DQ13	Data Input/Output
22	A1	Address	47	VSSQ	To Ground
23	A2	Address	48	DQ14	Data Input/Output
24	A3	Address	49	DQ15	Data Input/Output
25	VDD	Power Supply	50	VSS	To Ground

■ MN101C35DGD(IC701):System controller

Pin function

Pin No.	Symbol	I/O	Description
1	DDATA	O	DAC control data
2	DCLK	O	DAC control clock
3	DACOCS	O	DAC control chip select
4~7	DI/DO/CS/SK	-	Non connect
8	VDD	-	Power supply +B 5V
9	OSC2	O	Oscillation terminal 8MHz
10	OSC1	I	Oscillation terminal 8MHz
11	VSS	-	Connect to ground
12	XI	-	Unused, Connect with ground
13	XO	-	Unused
14	MMOD	-	Connect to ground
15	VREF-	-	Connect to ground
16	POWER SW	I	Key input (power)
17	NTSEL	I	NTSC/PAL switch input
18	RGB/YC SW	-	Un used
19	S/COMPO	-	Un used
20	AIN0	I	Key input (S831~S835)
21	AIN2	I	Key input (open/close)
22	TEST0	-	Un used
23	TEST1	-	Un used
24	VREF+	-	Power supply +B 5V
25	RGBSEL	O	RGB select control (H:RGB L:other)
26	RESET	I	Reset input
27	AVCO	O	AV COMPULINK output
28	AVCI	I	AV COMPULINK input
29	POWERON	O	Power ON output
30	TCLOSE	O	Tray close control output
31	YOPEN	O	Tray open control output
32	/LMMUTE	O	Tray muting output (L:muting)
33	SWOPEN	I	Detection switch of tray open/close (L:open/close)
34	SWUPDN	I	Detection switch of traverse mechanism up/down (H:UP L:DOWN)
35	REMO	I	Remote control interruption
36	NC	-	Non connect
37	REQ	I	Communication between unit microcomputers request
38	NC	-	Non connect
39	S2UDT	O	Communication between unit microcomputers DATA output
40	U2SDT	I	Communication between unit microcomputers DATA input
41	SCLK	O	Communication between unit microcomputers CLK
42	BUSY	O	Communication between unit microcomputers BUSY
43	CPURST	O	Unit microcomputers reset
44	NC	-	Non connect
45	VS3	O	S3 control (H:standby L:power ON)
46	VS1	O	S1 control
47	MUTE	O	Muting output
48	STANDBYIND	O	LED control signal output (standby)
49~51	NC	-	Non connect
52~64	1G~13G	O	FL grid control signal output
65~88	S1~S24	O	FL segment control signal output
89~99	NC	-	Non connect
100	VPP	-	-VDISP (apply -35V)

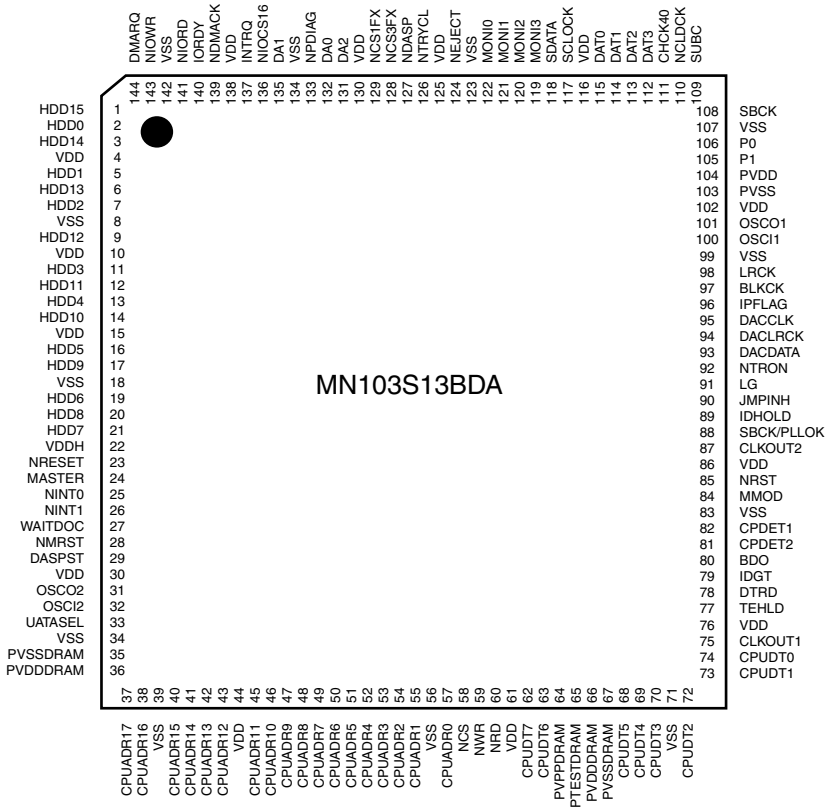
■ MN102L25GGE1(IC401):Unit CPU

Pin function

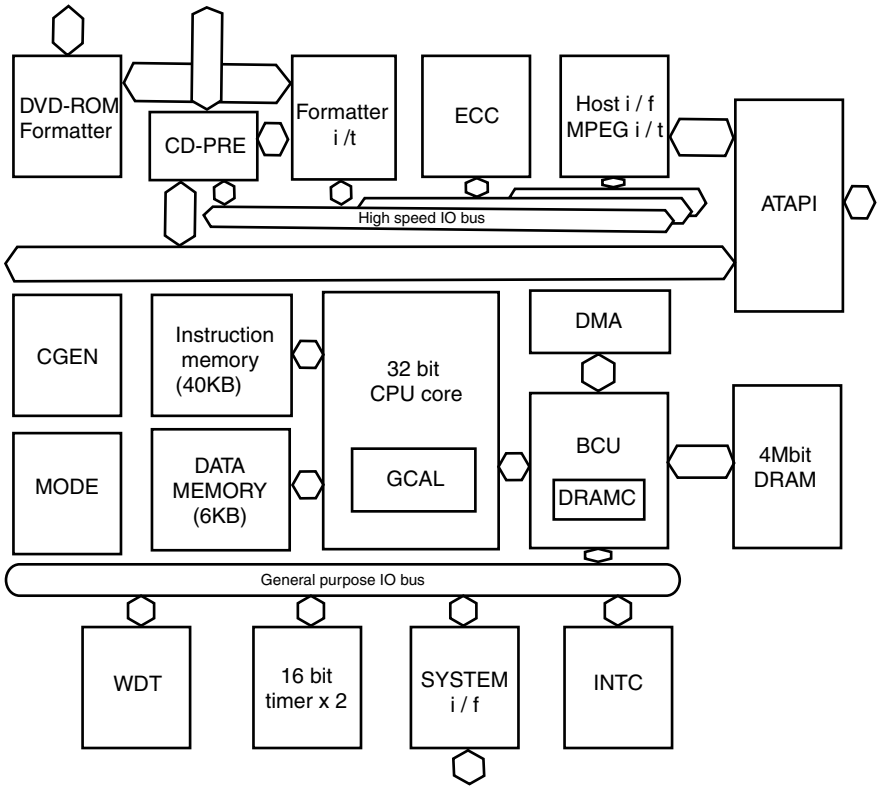
Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	WAIT	I	Micon wait signal input	51	-	-	
2	RE	O	Read enable	52	-	-	
3	SPMUTE	O	Spindle muting output to IC251	53	ADSCEN	O	Serial enable signal for ADSC
4	WEN	O	Write enable	54	VDD	-	Power supply
5	-	-	Non connect	55	FEPEN	O	Serial enable signal for FEP
6	CS1	O	Chip select for ODC	56	SLEEP	O	Standby signal for FEP
7	CS2	O	Chip select for ZIVA	57	BUSY	I	Communication busy
8	CS3	O	Chip select for outer ROM	58	REQ	O	Communication Request
9	DRVMUTE	O	Driver mute	59	CIRCEN	O	CIRC command select
10	SPKICK	O	Spin kick (Non connect)	60	-	-	Non connect
11	LSIRST	O	LSI reset	61	VSS	-	Ground
12	WORD	O	Bus selection input	62	EPCS	O	EEPROM chip select
13	A0	O	Address bus 0 for CPU	63	EPSK	O	EEPROM clock
14	A1	O	Address bus 1 for CPU	64	DPDI	I	EEPROM data input
15	A2	O	Address bus 2 for CPU	65	EPDO	O	EEPROM data output
16	A3	O	Address bus 3 for CPU	66	VDD	-	Power supply
17	VDD	-	Power supply	67	SCLKO	I	Communication clock
18	SYSCLK	O	System clock signal output	68	S2UDT	I	Communication input data
19	VSS	-	Ground	69	U2SDT	O	Communication output data
20	XI	-	Not use (Connect to vss)	70	CPSCK	O	Clock for ADSC serial
21	XO	-	Non connect	71	SDIN	I	ADSC serial data input
22	VDD	-	Power supply	72	SDOUT	O	ADSC serial data output
23	OSCI	I	Clock signal input(13.5MHz)	73	-	-	Not use
24	OSCO	O	Clock signal output(13.5MHz)	74	-	-	Not use
25	MODE	I	CPU Mode selection input	75	NMI	-	Not use
26	A4	O	Address bus 4 for CPU	76	ADSCIRQ	I	Interrupt input of ADSC
27	A5	O	Address bus 5 for CPU	77	ODCIRQ	I	Interrupt input of ODC
28	A6	O	Address bus 6 for CPU	78	DECIRQ	I	Interrupt input of ZIVA
29	A7	O	Address bus 7 for CPU	79	WAKEUP	O	Not use
30	A8	O	Address bus 8 for CPU	80	ODCIRQ2	I	Interruption of system control
31	A9	O	Address bus 9 for CPU	81	ADSEP	I	Address data selection input
32	A10	O	Address bus 10 for CPU	82	RST	I	Reset input
33	A11	O	Address bus 11 for CPU	83	VDD	-	Power supply
34	VDD	-	Power supply	84	TEST1	I	Test signal 1 input
35	A12	O	Address bus 12 for CPU	85	TEST2	I	Test signal 2 input
36	A13	O	Address bus 13 for CPU	86	TEST3	I	Test signal 3 input
37	A14	O	Address bus 14 for CPU	87	TEST4	I	Test signal 4 input
38	A15	O	Address bus 15 for CPU	88	TEST5	I	Test signal 5 input
39	A16	O	Address bus 16 for CPU	89	TEST6	I	Test signal 6 input
40	A17	O	Address bus 17 for CPU	90	TEST7	I	Test signal 7 input
41	A18	O	Address bus 18 for CPU	91	TEST8	I	Test signal 8 input
42	A19	O	Address bus 19 for CPU	92	VSS	-	Ground
43	VSS	-	Ground	93	D0	I/O	Data bus 0 of CPU
44	A20	O	Address bus 20 for CPU	94	D1	I/O	Data bus 1 of CPU
45	TXSEL	O	TX Select	95	D2	I/O	Data bus 2 of CPU
46	HAGUP	O		96	D3	I/O	Data bus 3 of CPU
47	-	-	Non connect	97	D4	I/O	Data bus 4 of CPU
48	-	-	Non connect	98	D5	I/O	Data bus 5 of CPU
49	HMFON			99	D6	I/O	Data bus 6 of CPU
50	TRVSW	I	Detection switch of traverse inside	100	D7	I/O	Data bus 7 of CPU

■ MN103S13BDA(IC301):Optical disc controller

1.Pin layout



2.Block diagram



3.Pin function (1/3)

Pin No.	Symbol	I/O	Description
1	HDD15	I/O	ATAPI Data
2	HDD0	I/O	ATAPI Data
3	HDD14	I/O	ATAPI Data
4	VDD	-	Power supply 3V
5	HDD1	I/O	ATAPI Data
6	HDD13	I/O	ATAPI Data
7	HDD2	I/O	ATAPI Data
8	VSS	-	Connect to GND
9	HDD12	I/O	ATAPI Data
10	VDD	-	Power supply 2.7V
11	HDD3	I/O	ATAPI Data
12	HDD11	I/O	ATAPI Data
13	HDD4	I/O	ATAPI Data
14	HDD10	I/O	ATAPI Data
15	VDD	-	Power supply 3V
16	HDD5	I/O	ATAPI Data
17	HDD9	I/O	ATAPI Data
18	VSS	-	Connect to GND
19	HDD6	I/O	ATAPI Data
20	HDD8	I/O	ATAPI Data
21	HDD7	I/O	ATAPI Data
22	VDDH		
23	NRESET	I	ATAPI Reset input
24	MASTER	I/O	ATAPI Master/slave select
25	NINT0	O	Interruption of system control 0
26	NINT1	O	Interruption of system control 1
27	WAITDOC	O	Wait control of system control
28	NMRST	O	Reset of system control (Connect to TP302)
29	DASPST	I	Setting of initial value of DASP signal
30	VDD	-	Power supply 3V
31	OSCO2	O	Non connect
32	OSCI2	I	Non connect
33	UATASEL	I	Connect to VSS
34	VSS	-	Connect to GND
35	PVSSDRAM		Connect to VSS
36	PVDDDRAM		Connect to VDD(2.7V)
37	CPUADR17	I	System control address
38	CPUADR16	I	System control address
39	VSS	-	Connect to GND
40	CPUADR15	I	System control address
41	CPUADR14	I	System control address
42	CPUADR13	I	System control address
43	CPUADR12	I	System control address
44	VDD	-	Power supply 2.7V
45	CPUADR11	I	System control address
46	CPUADR10	I	System control address
47	CPUADR9	I	System control address
48	CPUADR8	I	System control address
49	CPUADR7	I	System control address
50	CPUADR6	I	System control address

3.Pin function (2/3)

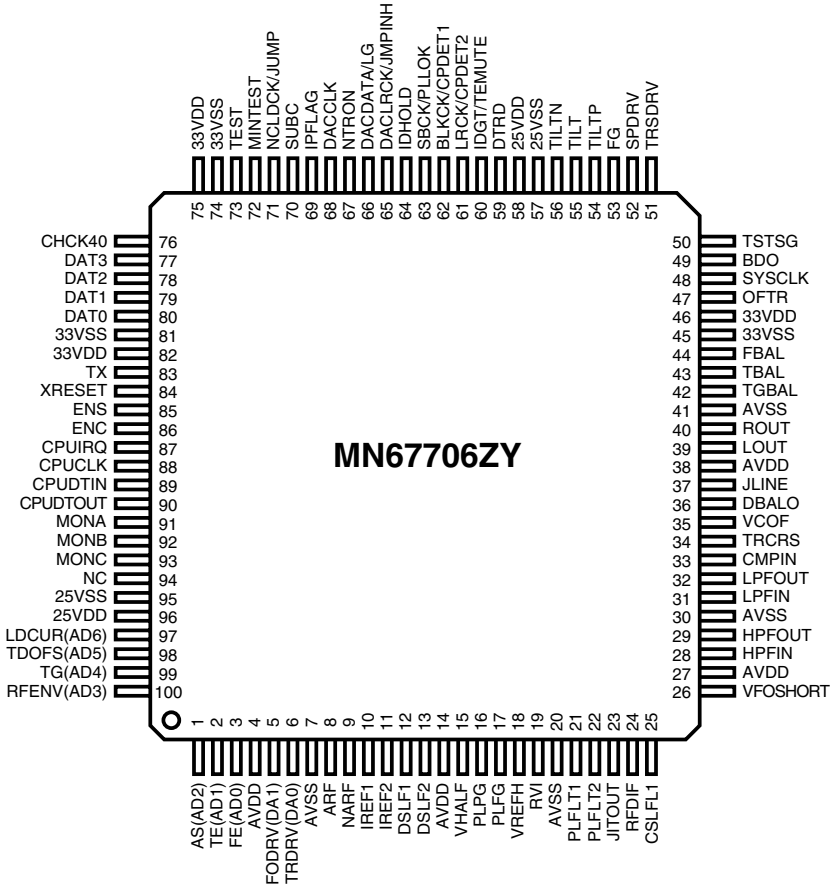
Pin No.	Symbol	I/O	Description
51	CPUADR5	I	System control address
52	CPUADR4	I	System control address
53	CPUADR3	I	System control address
54	CPUADR2	I	System control address
55	CPUADR1	I	System control address
56	VSS	-	Connect to GND
57	CPUADR0	I	System control address
58	NCS	I	System control chip select
59	NWR	I	Writing system control
60	NRD	I	Reading system control
61	VDD	-	Power supply 3V
62	CPUDT7	I/O	System control data
63	CPUDT6	I/O	System control data
64	PVPPDRAM	O	Connect to VSS
65	PTESTDRAM	I	Connect to VSS
66	PVDDDRAM		Connect to VDD(2.7V)
67	PVSSDRAM		Connect to VSS
68	CPUDT5	I/O	System control data
69	CPUDT4	I/O	System control data
70	CPUDT3	I/O	System control data
71	VSS	-	Connect to GND
72	CPUDT2	I/O	System control data
73	CPUDT1	I/O	System control data
74	CPUDT0	I/O	System control data
75	CLKOUT1	O	Clock signal output (16.9/11.2/8.45MHz)
76	VDD	-	Power supply 3V
77	TEHLD	O	Mirror gate (Connect to TP141)
78	DTRD	O	Data frequency control switch (Connect to TP304)
79	IDGT	O	CAPA switch
80	BDO	I	RF Dropout/BCA data
81	CPDET2	I	Outer capacity detection
82	CPDET1	I	Inner capacity detection
83	VSS	-	Connect to GND
84	MMOD	I	Connect to VSS
85	NRST	I	System reset
86	VDD	-	Power supply 3V
87	CLKOUT2	O	Clock 16.9MHz
88	SBCK/PLLOK	O	Flame mark detection
89	IDOHOLD	O	ID gate for tracking holding
90	JMPINH	O	Jump prohibition
91	LG	O	Land/group switch
92	NTRON	I	Tracking ON
93	DACDATA	O	Serial data output (Connect to TP148)
94	DACLRCK	O	Identification signal of L and R (Connect to TP149)
95	DACCLK	I	Clock for serial data output
96	IPFLAG	I	Input of IP flag
97	BLKCK	I	Sub code/block/input clock
98	LRCK	I	Identification signal of L and R (Connect to VSS)
99	VSS	-	Connect to GND
100	OSCI1	I	Oscillation input terminal 16.9MHz

3.Pin function (3/3)

Pin No.	Symbol	I/O	Description
101	OSCO1	O	Oscillation output terminal 16.9MHz
102	VDD	-	Power supply 3V
103	PVSS	-	Connect to GND
104	PVDD	-	Power supply 3V
105	P1	I/O	Terminal master polarity switch input
106	P0	I/O	CIRC-RAM,OVER/UNDER Interruption
107	VSS	-	Connect to GND
108	SBCK	O	Clock output for sub code,serial input
109	SUBC	I	Sub code,serial input
110	NCLDCK	I	Sub code,flame clock input
111	CHCK40	I	Clock is read to DAT3~0 (Output of division frequency from ADSC)
112	DAT3	I	Data is read from disc (Going side by side output from ADSC)
113	DAT2	I	Data is read from disc (Going side by side output from ADSC)
114	DAT1	I	Data is read from disc (Going side by side output from ADSC)
115	DAT0	I	Data is read from disc (Going side by side output from ADSC)
116	VDD	-	Power supply 3V
117	SCLOCK	I/O	Debug serial clock (270 ohm pull up)
118	SDATA	I/O	Debug serial data (270 ohm pull up)
119	MONI3	O	Internal good title monitor (Connect to TP150)
120	MONI2	O	Internal good title monitor (Connect to TP151)
121	MONI1	O	Internal good title monitor (Connect to TP152)
122	MONI0	O	Internal good title monitor (Connect to TP153)
123	VSS	-	Connect to GND
124	NEJECT	I	Eject detection
125	VDD	-	Power supply 2.7V
126	NTRYCL	I	Non connect (Tray close detection)
127	NDASP	I/O	ATAPI drive active / slave connect I/O
128	NCS3FX	I	Non connect (ATAPI host chip select)
129	NCS1FX	I	Non connect (ATAPI host chip select)
130	VDD	-	Power supply 3V
131	DA2	I/O	ATAPI host address
132	DA0	I/O	Non connect (ATAPI host address)
133	NPDIAG	I/O	ATAPI Slave master diagnosis input
134	VSS	-	Connect to GND
135	DA1	I/O	Non connect (ATAPI host address)
136	NIOCS16	O	Output of selection of width of ATAPI host data bus
137	INTRQ	O	ATAPI Host interruption output
138	VDD	-	Power supply 3V
139	NDMACK	I	Non connect (ATAPI Host DMA characteristic)
140	IORDY	O	ATAPI Host ready output (Connect to TP157)
141	NIORD	I	Non connect (ATAPI host read)
142	VSS	-	Connect to GND
143	NIOWR	I/O	ATAPI Host write
144	DMARQ	O	ATAPI Host DMA request (Connect to TP159)

■ MN67706ZY (IC201) : Auto digital servo controller

1.Terminal Layout



2.Pin Functions (1/3)

Pin No.	Symbol	I/O	Function
1	AS(AD2)	I	AS : Full adder signal(FEP)
2	TE(AD1)	I	Phase difference/3 beam tracking error(FEP)
3	FE(AD0)	I	Focus error(FEP)
4	AVDD	-	Apply 3.3V(For analog circuit)
5	FODRV(DA1)	O	Focus drive(DRVIC)
6	TRDRV(DA0)	O	Tracking drive(DRVIC)
7	AVSS	-	Ground(For analog circuit)
8	ARF	I	Equivalence RF+(FEP)
9	NARF	I	Equivalence RF-(FEP)
10	IREF1	I	Reference current1(For DBAL)
11	IREF2	I	Reference current2(For DBAL)
12	DSLF1	I/O	Connect to capacitor1 for DSL
13	DSLF2	I/O	Connect to capacitor2 for DSL
14	AVDD	-	Apply 3.3V(For analog circuit)
15	VHALF	I	Reference voltage 1.65+-0.1V(FEP)
16	PLPG	-	Not use(PLL phase gain setting resistor terminal)
17	PLFG	-	Not use(PLL frequency gain setting resistor terminal)
18	VREFH	I	Reference voltage 2.2V+-0.1V(FEP)
19	RVI	I/O	Connect to resistor for VREFH reference current source
20	AVSS	-	Ground(For analog circuit)
21	PLFLT1	O	Connect to capacitor1 for PLL
22	PLFLT2	O	Connect to capacitor2 for PLL
23	JITOUT	I/O	Output for jitter signal monitor
24	RFDIF	I	Not use
25	CSLFL1	I/O	Pull-up to VHALF

2.Pin function (2/3)

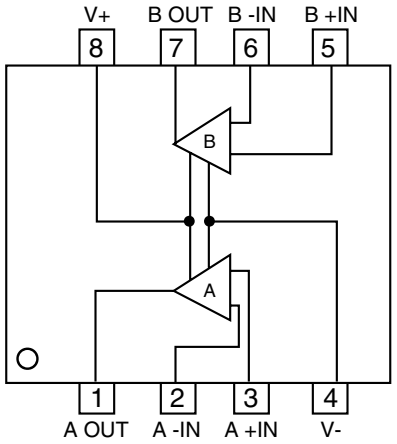
Pin No.	Symbol	I/O	Function
26	VFOSHORT	O	VFO short output
27	AVDD	-	Apply 3.3V(For analog circuit)
28	HPFIN	I	Pull-up to VHALF
29	HPFOUT	O	Connect to TP208
30	AVSS	-	Ground(For analog circuit)
31	LPFIN	I	Pull-up to VHALF
32	LPFOUT	O	Not use
33	CMPIN	I	Connect to TP210
34	TRCRS	I	Input signal for track cross formation
35	VCOF	I/O	JFVCO control voltage
36	DBALO	O	DSL balance adjust output
37	JLINE	O	J-line setting output(FEP)
38	AVDD	-	Apply 3.3V(For analog circuit)
39	LOUT	O	Connect to TP203 (Analog audio left output)
40	ROUT	O	Connect to TP204 (Analog audio right output)
41	AVSS	-	Ground(For analog circuit)
42	TGBAL	O	Tangential balance adjust(FEP)
43	TBAL	O	Tracking balance adjust(FEP)
44	FBAL	O	Focus balance adjust(FEP)
45	33VSS	-	Ground(For I/O)
46	33VDD	-	Apply 3.3V(For I/O)
47	OFTR	I	Off track signal
48	SYSCLK	I	16.9344MHz system clock input(ODC)
49	BDO	I	Drop out(FEP)
50	TSTSG	O	Calibration signal(FEP)
51	TRSDRV	O	Traverse drive(DRVIC)
52	SPDRV	O	Spindle drive output(DRVIC)
53	FG	I	FG signal input (Spindle motor driver)
54	TILTP	O	Connect to TP205
55	TILT	O	Connect to TP206
56	TILTN	O	Connect to TP207
57	25VSS	-	Ground(For internal core)
58	25VDD	-	Apply 2.5V(For internal core)
59	DTRD	I	Data read control signal(ODC)
60	IDGT/TEMUTE	I	Pull-down to Ground
61	LRCK/CPDET2	O	LR channel data strobe(ODC)/
62	BLKCK/CPDET1	O	CD sub code synchronous signal(ODC)/
63	SBCK/PLLOK	I	CD sub code data shift clock(ODC)/PLL pull-in OK signal input
64	IDHOLD	I	Pull-down to Ground
65	DACLRCK/JMPINH	I	1bit DAC-LR channel data strobe(ODC)/
66	DACDATA/LG	I	CD 1bit DAC channel data(ODC)
67	NTRON	O	L : Tracking ON(ODC)
68	DACCLK	O	1bit DAC channel data shift clock(ODC)
69	IPFLAG	O	CIRC error flag(ODC)
70	SUBC	O	CD sub code(ODC)
71	NCLDCK/JUMP	O	CD sub code data frame clock(ODC)/DVD JUMP signal(ODC)
72	MINTEST	I	Pull-down to Ground(For MINTEST)
73	TEST	I	Pull-down to Ground(For TEST)
74	33VSS	-	Ground(For I/O)
75	33VDD	-	Apply 3.3V(For I/O)
76	CHCK40	O	Clock for SRDATA(ODC)
77	DAT3	O	SRDATA3(ODC)
78	DAT2	O	SRDATA2(ODC)
79	DAT1	O	SRDATA1(ODC)
80	DAT0	O	SRDATA0(ODC)

2.Pin function (3/3)

Pin No.	Symbol	I/O	Function
81	33VSS	-	Ground(For I/O)
82	33VDD	-	Apply 3.3V(For I/O)
83	TX	O	Digital audio interface
84	XRESET	I	Reset input (System control)
85	ENS	I	Servo DSC serial I/F chip select (System control)
86	ENC	I	CIRC serial I/F chip select (System control)
87	CPUIRQ	O	Interrupt request (System control)
88	CPUCLK	I	Syscon serial I/F clock (System control)
89	CPUDTIN	I	Syscon serial I/F data input (System control)
90	CPUDTOUT	O	Syscon serial I/F data output (System control)
91	MONA	O	Connect to TP226 (Monitor terminal A)
92	MONB	O	Connect to TP225 (Monitor terminal A)
93	MONC	O	Connect to TP224 (Monitor terminal A)
94	NC	O	Connect to TP211
95	25VSS	-	Ground(For internal core)
96	25VDD	-	Apply 2.5V(For internal core)
97	LDCUR(AD6)	I	
98	TDOFS(AD5)	I	
99	TG(AD4)	I	Tangential phase difference(FEP)
100	RFENV(AD3)	I	RF envelope input(FEP)

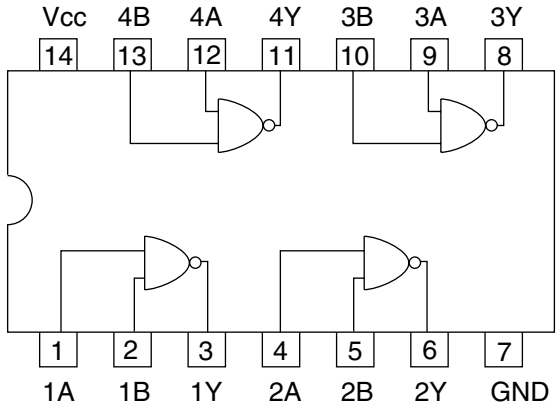
■ NJM4580M-X(IC741,IC751):Dual OP amplifier

Block diagram



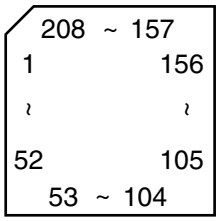
■ TC74VHC00FT-X(IC322,IC503) : Write timing control

1.Terminal layout / Block diagram



■ ZIVA-4.1-PA2(IC501):Back end - Digital decoder

1.Terminal layout



2.Pin function (1/5)

Pin No.	Symbol	I/O	Description
1	RD	I	Read strobe input
2	R/W	I	Read/write strobe input
3	VDD	-	Power supply terminal 3.3V
4	WAIT	O	Transfer not complete / data acknowledge. Active LOW to indicate host initiated transfer is complete.
5	RESET	I	Active LOW : reset signal input
6	VSS	-	Connect to ground
7	VDD	-	Power supply terminal 3.3V
8	INT	O	Host interrupt signal output
9	NC	-	Non connect
10	NC	-	Non connect
11	NC	-	Non connect
12	NC	-	Non connect
13	VDD	-	Power supply terminal 2.5V
14	VSS	-	Connect to ground
15	NC	-	Non connect
16	NC	-	Non connect
17	NC	-	Non connect
18	NC	-	Non connect
19	VSS	-	Connect to ground
20	VDD	-	Power supply 3.3V
21	VDATA0	O	Video data bus output. Byte serial CbYCrY data synchronous with VCLK.
22	VDATA1	O	Video data bus output. Byte serial CbYCrY data synchronous with VCLK.
23	VDATA2	O	Video data bus output. Byte serial CbYCrY data synchronous with VCLK.
24	VDATA3	O	Video data bus output. Byte serial CbYCrY data synchronous with VCLK.
25	VDATA4	O	Video data bus output. Byte serial CbYCrY data synchronous with VCLK.
26	VDATA5	O	Video data bus output. Byte serial CbYCrY data synchronous with VCLK.
27	VDATA6	O	Video data bus output. Byte serial CbYCrY data synchronous with VCLK.
28	VDATA7	O	Video data bus output. Byte serial CbYCrY data synchronous with VCLK.
29	VSYNC	I/O	Vertical sync. Bi-directional, the decoder output the top border of a new field on the first HSYNC after the falling edge of VSYNC.
30	HSYNC	I/O	Horizontal sync. The decoder begins outputting pixel data for a new horizontal line after the falling (active) edge of HSYNC.
31	VSS	-	Connect to ground
32	VDD	-	Power supply terminal 3.3V
33	NC	-	Non connect
34	NC	-	Non connect
35	NC	-	Non connect
36	VDD	-	Power supply terminal 2.5V

2.Pin function (2/5)

Pin No.	Symbol	I/O	Description
37	VSS	-	Connect to ground
38	NC	-	Non connect
39	NC	-	Non connect
40	NC	-	Non connect
41	NC	-	Non connect
42	NC	-	Non connect
43	PIO0	I/O	Programmable I/O terminal
44	VSS	-	Connect to ground
45	VDD	-	Power supply terminal 3.3V
46	PIO1	I/O	Programmable I/O terminal
47	PIO2	I/O	Programmable I/O terminal
48	PIO3	I/O	Programmable I/O terminal
49	PIO4	I/O	Programmable I/O terminal
50	PIO5	I/O	Programmable I/O terminal
51	PIO6	I/O	Programmable I/O terminal
52	PIO7	I/O	Programmable I/O terminal
53	MDATA0	I/O	SDRAM data
54	MDATA1	I/O	SDRAM data
55	VDD	-	Power supply terminal 3.3V
56	VSS	-	Connect to ground
57	MDATA2	I/O	SDRAM data
58	MDATA3	I/O	SDRAM data
59	MDATA4	I/O	SDRAM data
60	MDATA5	I/O	SDRAM data
61	MDATA6	I/O	SDRAM data
62	MDATA7	I/O	SDRAM data
63	MDATA15	I/O	SDRAM data
64	VDD	-	Power supply terminal 3.3V
65	VSS	-	Connect to ground
66	MDATA14	I/O	SDRAM data
67	VDD	-	Power supply terminal 2.5
68	VSS	-	Connect to ground
69	MDATA13	I/O	SDRAM data
70	MDATA12	I/O	SDRAM data
71	MDATA11	I/O	SDRAM data
72	MDATA10	I/O	SDRAM data
73	MDATA9	I/O	SDRAM data
74	VDD	-	Power supply terminal 3.3V
75	VSS	-	Connect to ground
76	MDATA8	I/O	SDRAM data
77	LDQM	O	SDRAM Lower or upper mask
78	SD-CLK	O	SDRAM Clock
79	CLKSEL	I	Selects SYSCLK or VCLK as clock source. Normal operation is to tie HIGH.
80	MADDR9	O	SDRAM address
81	MADDR8	O	SDRAM address
82	VDD	-	Power supply terminal 3.3V
83	VSS	-	Connect to ground
84	MADDR7	O	SDRAM address

2.Pin function (3/5)

Pin No.	Symbol	I/O	Description
85	MADDR6	O	SDRAM address
86	MADDR5	O	SDRAM address
87	VDD	-	Power supply terminal 2.5V
88	VSS	-	Connect to ground
89	MADDR4	O	SDRAM address
90	MWE	O	SDRAM write enable
91	SD-CAS	O	Active LOW SDRAM column address
92	VDD	-	Power supply terminal 3.3V
93	VSS	-	Connect to ground
94	SD-RAS	O	Active LOW SDRAM row address
95	SD-CS0	O	Active LOW SDRAM chip select 0
96	SD-CS1/MADDR11	O	Active LOW SDRAM chip select 1 or use as MADDR11 for larger SDRAM
97	SD-BS	O	SDRAM bank select
98	MADDR10	O	SDRAM address
99	MADDR0	O	SDRAM address
100	VDD	-	Power supply terminal 3.3V
101	VSS	-	Connect to ground
102	MADDR1	O	SDRAM address
103	MADDR2	O	SDRAM address
104	MADDR3	O	SDRAM address
105	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table1
106	NC	-	Non connect
107	NC	-	Non connect
108	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table1
109	NC	-	Non connect
110	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table1
111	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table1
112	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table1
113	DAI-LRCK	I	PCM left/right clock
114	DAI-BCK	I	PCM input bit clock
115	VDD	-	Power supply 3.3V
116	VSS	-	Connect to ground
117	DAI-DATA	I	PCM data input
118	DA-DATA3	O	PCM data output. Eight channels. Serial audio samples relative to DA_BCK and DA_LRCK
119	DA-DATA2	O	PCM data output. Eight channels. Serial audio samples relative to DA_BCK and DA_LRCK
120	DA-DATA1	O	PCM data output. Eight channels. Serial audio samples relative to DA_BCK and DA_LRCK
121	DA-DATA0	O	PCM data output. Eight channels. Serial audio samples relative to DA_BCK and DA_LRCK
122	DA-LRCK	O	PCM left clock. Identifies the channel for each sample
123	VDD	-	Power supply terminal 3.3V
124	VSS	-	Connect to ground
125	DA-XCK	I/O	Audio external frequency clock input or output
126	DA-BCK	O	PCM bit clock output
127	DA-IEC	O	PCM data out in IEC-958 format or compressed data out in IEC-1937 format
128	VDD	-	Power supply terminal 2.5V

2.Pin function (4/5)

Pin No.	Symbol	I/O	Description
129	VSS	-	Connect to ground
130	NC	-	Non connect
131	VSS_DAC	-	Connect to ground for analog video DAC
132	VSS_VIDEO	-	Connect to ground for analog video
133	CVBS	O	DAC video output format : CVBS. Macrovision encoded
134	VDD_DAC	-	Power supply terminal for analog video DAC
135	VDD_VIDEO	-	Power supply terminal for analog video
136	NC	-	Non connect
137	VSS_DAC	-	Connect to ground for analog video DAC
138	VSS_VIDEO	-	Connect to ground for analog video
139	CVBS/G/Y	O	DAC video output format. Macrovision encoded
140	VDD_DAC	-	Power supply terminal for analog video DAC
141	VDD_VIDEO	-	Power supply terminal for analog video
142	NC	-	Non connect
143	VSS_DAC	-	Connect to ground for analog video DAC
144	VSS_VIDEO	-	Connect to ground for analog video
145	Y/B/U	O	DAC video output format. Macrovision encoded
146	VDD_DAC	-	Power supply terminal for analog video DAC
147	VDD_VIDEO	-	Power supply terminal for analog video
148	NC	-	Non connect
149	VSS_DAC	-	Connect to ground for analog video DAC
150	VSS_VIDEO	-	Connect to ground for analog video
151	C/R/V	O	DAC video output format. Macrovision encoded
152	VDD_DAC	-	Power supply terminal for analog video DAC
153	VDD_VIDEO	-	Power supply terminal for analog video
154	VSS_RREF	-	Connect to ground for analog video
155	RREF	O	Reference resistor. Connecting to pin 154
156	VDD_RREF	-	Power supply terminal for analog video 3.3V
157	A_VSS	-	Power supply terminal for analog PLL 3.3V
158	SYSCLK	I	Optical system clock. Tie to A_VDD through a 1K ohm resistor
159	VCLK	I	System clock input
160	A_VDD	-	Power supply terminal for analog PLL 3.3V
161	DVD-DATA0/CD-DATA	I	Serial CD data. This pin is shared with DVD compressed data DVD-DATA0
162	DVD-DATA1/CD-LRC	I	Programmable polarity 16-bit word synchronization to the decoder. This pin is shared with DVD compressed data DVD-DATA1
163	DVD-DATA2/CD-BCK	I	CD bit clock. Decoder accept multiple BCK rates. This pin is shared with DVD compressed DVD-DATA2
164	DVD-DATA3/CD-C2PO	I	Asserted HIGH indicates a corrupted byte. This pin is shared with DVD compressed data DVD-DATA3
165	DVD-DATA4/CDGSDATA	I	DVD parallel compressed data from DVD DSP. or CD-G data indicating serial subcode data input
166	VSS	-	Connect to ground
167	VDD	-	Power supply terminal 3.3V
168	DVD-DATA5/CDG-VFSY	I	DVD parallel compressed data from DVD DSP. or CD-G frame sync indicating frame-start or composite synchronization input.
169	DVD-DATA6/CDG-SOS1	I	DVD parallel compressed data from DVD DSP. or CD-G block sync indicating block-start synchronization input

2.Pin function (5/5)

Pin No.	Symbol	I/O	Description
170	DVD-DATA7/CDG-SCLK	I	DVD parallel compressed data from DVD DSP. or CD-G clock indicating sub code data clock input or output
171	VDACK	I	In synchronous mode, bitstream data acknowledge. Asserted when DVD data is valid.Polarity is programmable
172	VREQUEST	O	Bitstream request
173	VSTROBE	I	Bitstream strobe
174	ERROR	I	Error in input data
175	VDD	-	Power supply terminal 3.3V
176	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
177	VDD	-	Power supply terminal 3.3V
178	VSS	-	Connect to ground
179	NC	-	Non connect
180	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
181	NC	-	Non connect
182	HADDR0	I	Host addressbus. 3-bit address bus selects one of eight host interface registers
183	HADDR1	I	Host addressbus. 3-bit address bus selects one of eight host interface registers
184	HADDR2	I	Host addressbus. 3-bit address bus selects one of eight host interface registers
185	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
186	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
187	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
188	VSS	-	Connect to ground
189	VDD	-	Power supply terminal 2.5V
190	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
191	VSS	-	Connect to ground
192	VDD	-	Power supply terminal 3.3V
193	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
194	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
195	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
196	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
197	HDATA7	I/O	The 8-bit bi-derectional host data through which the host writes data to the decoder code.
198	VSS	-	Connect to ground
199	HDATA6	I/O	The 8-bit bi-derectional host data through which the host writes data to the decoder code.
200	HDATA5	I/O	The 8-bit bi-derectional host data through which the host writes data to the decoder code.
201	HDATA4	I/O	The 8-bit bi-derectional host data through which the host writes data to the decoder code.
202	HDATA3	I/O	The 8-bit bi-derectional host data through which the host writes data to the decoder code.
203	HDATA2	I/O	The 8-bit bi-derectional host data through which the host writes data to the decoder code.
204	VDD	-	Power supply terminal 3.3V
205	VSS	-	Connect to ground
206	HDATA1	I/O	The 8-bit bi-derectional host data through which the host writes data to the decoder code.
207	HDATA0	I/O	The 8-bit bi-derectional host data through which the host writes data to the decoder code.
208	CS	I	Host chip select input

JVC

VICTOR COMPANY OF JAPAN, LIMITED
OPTICAL DISC BUSINESS DIV. PERSONAL & MOBILE NETWORK BUSINESS UNIT
AV & MULTIMEDIA COMPANY 1644, Shimotsuruma, Yamato, Kanagawa 242-8514, Japan

No.A0003

Printed in Japan
200102(S)